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Evaluation of Fault Current Contribution Strategies by Converter Based Distributed Generation

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Dissertation presented in partial fulfilment of the requirements for the degree of PhD in Engineering Science: Electrical Engineering

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Abstract

It is a clear trend that the share of Distributed Generation (DG) in the grid increases. Many DG units are Converter Based DG (CBDG) units and it is expected that the number of CBDG units will increase in the future. Due to the variable nature of most of these CBDG units, there will be occasions when the share of CBDG units is much higher than their average share in the energy production. During these periods, several of the conventional synchronous generators will be disconnected from the grid and scenarios with a large number of CBDG units and very few synchronous generators arise.

The goal of this dissertation is to evaluate the impact of these scenarios on the fault currents and voltages during balanced and unbalanced faults. On the one hand, fault currents have a direct impact on the protection system of the grid. On the other hand, the grid voltages during a fault determine the impact of the fault on the loads and the generation units. Therefore, both the fault currents and fault voltages strongly influence the reliability of the grid.

First, it is demonstrated that existing control systems of CBDG units are able to flexibly control the fault current injections of CBDG units. Thus, their fault behaviour is a design parameter. Several specific control aspects related to the injection of negative sequence currents during faults are explained.

Since detailed electromagnetic transient simulations are considered computationally too intensive for scenarios with multiple CBDG units, this dissertation investigates which simplified method is able to evaluate the fault currents and fault voltages in these scenarios. As the fault behaviour of CBDG units is a design parameter, it is clear that any method has to take into account the control objectives of the CBDG units. Based on these requirements, a simplified calculation framework is developed and validated. This framework is then used to evaluate different current contribution strategies during balanced and unbalanced faults in scenarios with a high share of CBDG.

For balanced faults, the influence of different voltage support settings on the

short-circuit power in the grid is investigated. It is shown that CBDG units, with the appropriate voltage support settings, can contribute to the short-circuit power of the grid. This way, the CBDG units limit the drop in short-circuit power at the higher voltage levels when they replace conventional generation. When this reduction of the short-circuit power at the higher voltage levels is limited, the fault currents at the lower voltage levels, supplied by the higher voltage levels, do not change significantly. This avoids a complete redesign of the existing protection systems of typical European medium and low voltage grids in scenarios with a high share of CBDG and little conventional generation, as these protection systems rely on the magnitude of the fault currents. Locally, the voltage support of CBDG units can result in a (limited) increase of the short-circuit power. The voltage support can then be applied until the short-circuit power limits of the local grid are reached.

For unbalanced faults, scenarios with a high share of CBDG and little conventional generation are evaluated. When only positive sequence voltage support is applied, and negative sequence currents are blocked by the CBDG units, this can lead to very low fault currents during unbalanced faults. These low fault currents would require a complete redesign, including huge investment costs, of the existing protection systems at the lower voltage levels of the grid, as these protection systems rely on the magnitude of the fault currents. In addition, very low fault currents result in a reduced reliability of the grid, as faults at lower voltage levels then have a significant impact on the higher voltage levels. The remaining synchronous generators in the grid also experience additional stress when CBDG units only provide positive sequence voltage support during unbalanced faults. When CBDG units provide both positive and negative sequence voltage support, these drawbacks are avoided: the existing protection systems of typical European medium and low voltage grids do not require a complete redesign, faults on the lower voltage levels do not have a significant impact on the higher voltage levels and the remaining synchronous generators don't experience additional stress.

Beknopte samenvatting

Er is een duidelijke trend naar meer gedistribueerde elektriciteitsopwekking. Hierdoor stijgt het aandeel van de gedistribueerde bronnen in de elektriciteitsnetten ten opzichte van de conventionele generatoren. Veel van deze gedistribueerde bronnen zijn vermogenelektronische bronnen en men verwacht nog een toename van vermogenelektronische gedistribueerde bronnen in de toekomst. Door hun zeer variabele energieopwekking zullen er ook periodes zijn wanneer het ogenblikkelijke aandeel van vermogenelektronische gedistribueerde bronnen veel hoger is dan hun gemiddeld aandeel in de energieproductie. Tijdens die periodes worden verschillende conventionele generatoren uit dienst genomen. Dit resulteert in scenario's met veel vermogenelektronische gedistribueerde bronnen en weinig synchrone generatoren.

Deze doctoraatsthesis onderzoekt de invloed van deze scenario's op foutstromen en spanningen tijdens gebalanceerde en ongebalanceerde fouten. Zowel de foutstromen als de foutspanningen beïnvloeden de betrouwbaarheid van het net. De foutstromen in een net hebben namelijk een rechtstreekse invloed op het beveiligingssysteem van het net, terwijl de spanningen tijdens een fout de gevolgen van de fout voor de lasten en de generatoren bepalen.

Eerst wordt aangetoond dat de bestaande regelsystemen voor vermogenelektronische gedistribueerde bronnen in staat zijn om de foutstroombijdragen van deze bronnen te bepalen. Het foutgedrag van deze bronnen is dus een ontwerpparameter. Verschillende regelaspecten van inverse stroombijdragen tijdens fouten worden ook behandeld.

Aangezien gedetailleerde elektromagnetische simulaties (EMT-simulaties) te rekenintensief zijn om scenario's met veel vermogenelektronische gedistribueerde bronnen te evalueren, onderzoekt deze doctoraatsthesis welke vereenvoudigde berekeningsmethoden de foutstromen en foutspanningen kunnen bepalen. Aangezien het gedrag van de vermogenelektronische gedistribueerde bronnen een ontwerpparameter is, dient elke berekeningsmethode rekening te houden

met de regeldoelstellingen. Op basis van deze vereiste is een vereenvoudigde berekeningsmethode ontwikkeld en gevalideerd. Deze methode is vervolgens gebruikt om verschillende foutstroombijdragen van vermogenelektronische gedistribueerde bronnen te evalueren in scenario's waar deze bronnen instaan voor een groot deel van de elektriciteitsopwekking.

Voor gebalanceerde fouten onderzoekt dit werk de invloed van verschillende instellingen voor de spanningsondersteuning op het kortsluitvermogen van het net. Hieruit blijkt dat vermogenelektronische gedistribueerde bronnen kunnen bijdragen tot het kortsluitvermogen van het net, mits ze de geschikte instellingen voor de spanningsondersteuning hebben. Zo beperken deze bronnen de daling van het kortsluitvermogen op de hoogste spanningsniveaus wanneer ze conventionele generatoren vervangen. Bij een beperkte daling van het kortsluitvermogen op de hoogste spanningsniveaus wijzigen de foutstromen, geleverd door de hogere spanningsniveaus naar fouten op lagere spanningsniveaus, nauwelijks. Dit vermijdt dat de bestaande beveiligingssystemen van typische Europese midden- en laagspanningsnetten volledig herontworpen moeten worden, gezien deze beveiligingssystemen gebaseerd zijn op de grootte van deze foutstromen. Lokaal kan het kortsluitvermogen (beperkt) toenemen door de spanningsondersteuning van vermogenelektronische gedistribueerde bronnen. Deze spanningsondersteuning kan dan toegepast worden tot de kortsluitvermogenlimieten van het lokale net bereikt zijn.

Voor ongebalanceerde fouten zijn scenario's onderzocht met veel vermogenelektronische gedistribueerde bronnen en weinig synchrone generatoren. Wanneer alleen spanningsondersteuning in het directe systeem toegepast wordt en de stromen in het inverse systeem onderdrukt worden, kan dit resulteren in zeer lage foutstromen. Deze lage foutstromen zouden een herontwerp, met de bijbehorende enorme investeringen, van de bestaande beveiligingssystemen op de laagste spanningsniveaus vereisen. Deze beveiligingssystemen zijn immers gebaseerd op de grootte van de foutstromen. Bovendien resulteren de zeer lage foutstromen in een daling van de betrouwbaarheid van het net, want fouten op de lagere spanningsniveaus hebben dan een aanzienlijke invloed op de hogere spanningsniveaus. De overblijvende synchrone generatoren ervaren ook extra stress wanneer de vermogenelektronische gedistribueerde bronnen alleen spanningsondersteuning in het directe systeem bieden tijdens ongebalanceerde fouten. Wanneer de vermogenelektronische gedistribueerde bronnen zowel spanningsondersteuning in het directe als in het inverse systeem bieden, zijn deze nadelen niet aanwezig: de bestaande beveiligingssystemen van typische Europese midden- en laagspanningsnetten moeten niet volledig gewijzigd worden, fouten op de lagere spanningsniveaus hebben geen grote invloed op de hogere spanningsniveaus en overblijvende synchrone generatoren ervaren geen extra stress.

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> "As with so many things in life,
> the joy of finding Waldo is in the
> journey, not the destination."
> — Randy Olson.

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Thomas Wijnhoven
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List of Abbreviations

AC	Alternating Current
ANSI	American National Standards Institute
AVM	Averaged Value Model
AVR	Automatic Voltage Regulator
CBDG	Converter Based Distributed Generation
CHP	Combined Heat and Power
CSC	Current Source Converter
DB	DeadBand
DC	Direct Current
DDSRF	Decoupled Double Synchronous Reference Frame
DFIG	Doubly-Fed Induction Generator
DG	Distributed Generation
DSO	Distribution System Operator
DSRF	Double Synchronous Reference Frame
DT	Distribution Transformer
EMT	ElectroMagnetic Transient
EU	European Union
FACTS	Flexible AC Transmission Systems
FRT	Fault Ride Through
GSC	Grid Side Converter
HV	High Voltage
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IG	Induction Generator
IGBT	Insulated Gate Bipolar Transistor
ILNEM	Iterative Linear Network Equations Method
LV	Low Voltage
MPPT	Maximum Power Point Tracking
MSC	Machine Side Converter

MV	Medium Voltage
NPC	Neutral-Point Clamped
PCC	Point of Common Coupling
PI	Proportional Integral
PLL	Phase Locked Loop
PR	Proportional Resonant
PT	Power Transformer
p.u.	per unit
PV	PhotoVoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
SG	Synchronous Generator
SRF	Synchronous Reference Frame
SVM	Space Vector Modulation
TSO	Transmission System Operator
VSC	Voltage Source Converter
WECC	Western Electricity Coordinating Council
WPP	Wind Power Plant
WRIG	Wound-Rotor Induction Generator
WT	Wind Turbine

List of Symbols

Symbol	Description
B	Susceptance
C	Capacitance
E (e)	Internal voltage source of synchronous machine (p.u.)
f	Frequency
$\mathrm{f}_{\mathrm{carrier}}$	Switching frequency
H	Inertia constant
I (i)	Current (p.u.)
k	Gain of the voltage support
L	Inductance
P (p)	Active power (p.u.)
P_0 (p_0)	Average active power (p.u.)
P_{c2} (p_{c2})	Double frequency active power term 1 (p.u.)
P_{s2} (p_{s2})	Double frequency active power term 2 (p.u.)
P_{var} (p_{var})	Total double frequency active power term (p.u.)
Q (q)	Reactive power (p.u.)
Q_0 (q_0)	Average reactive power (p.u.)
R (r)	Resistance (p.u.)
S (s)	Apparent power (p.u.)
S_{sc}	Short-circuit power
t	Time
T	Time constant
U (u)	Voltage (p.u.)

u_k	Impedance voltage
u_{k0}	Zero sequence impedance voltage
u_r	Ohmic part of impedance voltage
X (x)	Reactance (p.u.)
z_{0HL}	Zero sequence impedance, looking into winding H with winding M open
z'_{0H}	Zero sequence impedance, looking into winding H with winding M short-circuited
z_{0ML}	Zero sequence impedance, looking into winding M with winding L open
z_{1HM}	Positive sequence impedance, looking into winding H with winding M open
Δ	Delta (difference between two values)
ω	Angular frequency
ω_1	Angular frequency of the positive sequence voltage
ω_2	Angular frequency of the negative sequence voltage
ω_2^*	Angular frequency of the complex conjugate negative sequence voltage
θ_1	Angle of the positive sequence voltage
θ_2	Angle of the negative sequence voltage
θ_2^*	Angle of the complex conjugate negative sequence voltage

Subscript	**Description**
0	Zero sequence value (or when specified: prefault value)
1	Positive sequence value
2	Negative sequence value
a	Phase a value
b	Phase b value
c	Phase c value
CBDG	CBDG value
d	d-axis component (rotating reference frame)
DC	DC value

dyn	Dynamic value
eq	Equivalent value
F	Filter value
fault	Fault value
grid	Grid value
GSC	GSC value
lim	Limit value
line	Line value
load	Load value
max	Maximal value
meas	Measured value
min	Minimal value
MSC	MSC value
nom	Nominal (rated) value
PV	PV value
prefault	Prefault value
prim	Primary side value
q	q-axis component (rotating reference frame)
red	Reduction value
ref	Reference value / setpoint
sc	Short-circuit value
sec	Secondary side value
source	Source value
steady state	Steady state value
tot	Total value
T	Transformer value
V	Virtual value
VSC	VSC value
α	α-axis component (stationary reference frame)
β	β-axis component (stationary reference frame)
$\underline{\ }$	Phasor (underlined)

Superscript	**Description**
$\angle$	Space vector
$\angle 0$	Space vector in stationary $\alpha\beta$ frame
$\angle\theta$	Space vector in reference frame aligned to angle θ
$*$	Complex conjugate
$'$	Transient value
$''$	Subtransient value

Chapter 1

Introduction

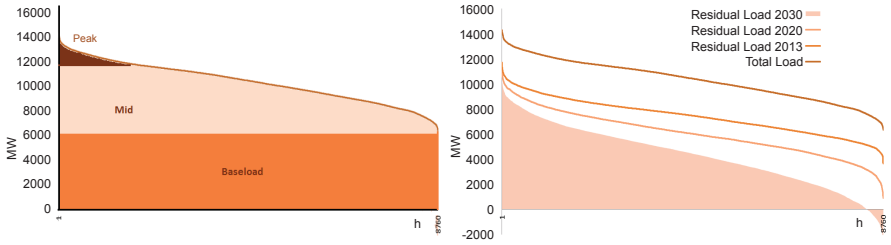
"The real questions are: Does it solve a problem? Is it serviceable? How is it going to look in ten years?"

— Charles Eames.

1.1 Context

1.1.1 Increasing Share of (Converter Based) Distributed Generation

Today it is generally accepted that the share of Distributed Generation (DG) will continue to rise. There are several reasons for this increase: the increasing renewable energy targets and the decreasing CO_2 emission allowances set by the European Union (EU) [1], the decrease in costs of DG [2–4], the rising awareness of limited resources, ... Due to their nature (PhotoVoltaic (PV)) or due to technical advantages (type 4 Wind Turbine (WT)) more and more of these sources are connected through a full power electronic interface. The primary source of energy is converted to a Direct Current (DC) bus and then this DC bus is connected to the grid through a power electronic converter. These units are called Converter Based Distributed Generation (CBDG). This dissertation focuses on CBDG and scenarios where most DG units are of this type. Other DG units can be connected through a Synchronous Generator (SG),



(a) (b)

Figure 1.1: Evolution of the monotone residual load for the Elia control zone (source: [6]): (a) in 2000 and (b) in 2030

an Induction Generator (IG) or through a Doubly-Fed Induction Generator (DFIG).

The share of DG units in the grid can be expressed in terms of their share in the total energy generation (like the well-known EU 2020 targets or the 27% target in 2030 [1]). According to [5], there is a large difference between the European countries. In 2014, the share of wind and solar energy in Europe was 14.4%, while this was 4.2% for France, 10.8% for Belgium, 16.4% for Germany, 21.2% for Ireland, 24% for Spain and 44.6% for Denmark [5]. In addition, due to the large variability in the system, there are times when the share of DG units is much higher. The Belgian Transmission System Operator (TSO) Elia foresees that the share of residual load, i.e. the part of the total load that can be managed by TSO-controlled generation[1], will change significantly over the coming years. Figure 1.1 shows that in 2000, there was always a significant amount of baseload in the system: typically served by large SGs. In 2030, it is foreseen that there will be periods when there is a negative residual load for some hours of the year [6].

This does not mean that there are no SGs in the system. There can be some smaller SGs in Distribution System Operator (DSO) grids and some larger units may continue to exist. However, these larger units are not required to operate from a load point of view. In case of export to other countries, they can also remain operational. In addition, other SGs are connected to the system through the interconnection of the European grid. Nevertheless, there will be fewer large units in the system and much more DG units. When this evolution continues, this trend will increase: fewer SGs and more DG units during longer periods.

[1]So in fact, this residual load is the load that has to be fed by conventional SGs (i.e. the generation exclusive of decentralised generation (Combined Heat and Power (CHP)) in DSO grids and all wind & PV generation).

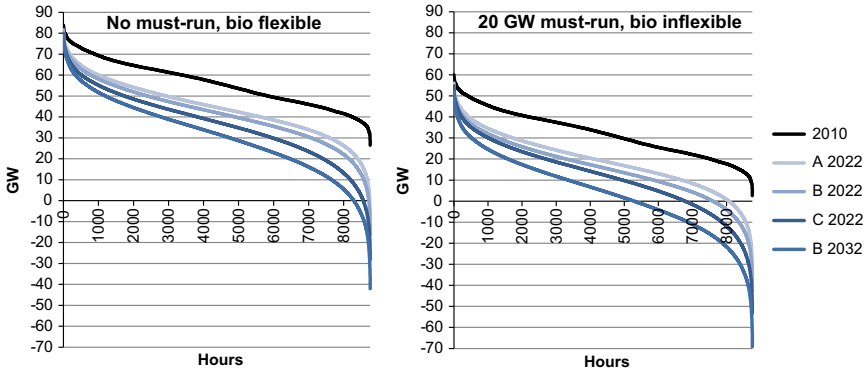


Figure 1.2: Residual load in Germany for several NEP (Netzentwicklungsplan) scenarios (source: [7])

Similar analyses are valid for other regions. Figure 1.2 shows the residual load curves for Germany under several grid development plans (NEP = Netzentwicklungsplan Strom 2012, [7,8]). It is clear that under the various scenarios the same trend as in Figure 1.1 is noticed.

Given this information, it is clear that there will be occasions in the future when the grids will operate with a high share of DG in the system. The next section will focus on the CBDG.

Converter Based Distributed Generation

There are several types of DG units. When the primary source is considered, there are thermal sources (e.g. CHP), hydro sources (e.g. tidal energy), solar sources (e.g. PV) and wind sources (e.g. WTs).

Thermal sources are usually connected to a motor or turbine that converts the thermal energy into motion. This motion then drives a generator (IG or SG). Because the motor or turbine can be optimally designed to run at constant speed, the direct connection of the motor/turbine and generator with the grid, operating at constant frequency, is not a problem. These types of generation sources are usually not converter based. One exception to this are the microturbines [9]. These gas driven turbines usually operate at very high rotational speeds (50000-120000 rpm) and the output of the generator is converted through power electronics. This power electronic connection also increases the usability of the sources when they have to work without the grid (island mode). In conclusion, for now most of the thermal sources are not

converter based, but in the future some of these DG units can be converter based.

Hydro sources are usually connected to the grid with a hydraulic turbine and then a SG. Newer (small) hydro power sources can also be connected through converters [9], but their share is currently very limited.

Solar sources are mainly PV units, although other forms (e.g. concentrated solar power thermal generation) exist. Until recently, it was the most rapidly growing form of DG in Europe and it has made the highest progress in terms of costs [10]. More recently, the yearly growth rates have decreased [5, 10]. The PV units generate DC power that is converted to Alternating Current (AC) power through a converter. All PV units are thus by definition converter based.

Wind sources mainly consist of horizontal axis WTs, although other concepts (e.g. vertical axis WTs) exist [9]. Horizontal axis WTs, from now on simply WTs, are classified into four types [11, 12]. Type 1 and 2 WTs are directly connected to the grid through an IG or a Wound-Rotor Induction Generator (WRIG). In Europe, most new WTs are either type 3 WTs with a DFIG or type 4 WTs with a (permanent magnet) SG and a full converter interface [13]. DFIGs use only a partially rated power electronic converter to supply the rotor of the induction generator. They represent a very interesting technology and currently most of the installed capacity of WTs are of this type [13, 14]. Estimates for the total installed capacity in 2010, show a market share for Europe of 55% for type 3 WTs compared to 25% for type 4 WTs. In addition, new installations are almost exclusive type 3 or type 4 WTs [13]. Worldwide estimates show a somewhat larger share of type 1 WTs. It is expected that the share of type 4 WTs will increase further in Europe [14]. Decreasing costs of power electronics can reinforce this trend. This work focuses exclusively on Converter Based Distributed Generation (CBDG) and therefore excludes the analysis of type 3 WTs. There also exists very interesting work on DFIGs and their fault behaviour. Therefore, when appropriate, references to this work on type 3 WTs will be given.

Another recent trend is storage. Due to the variability of many new generation sources, storage options become more attractive. Common storage options, e.g. pumped hydro generation, use conventional generators. However, the rising interest in battery storage also means new storage is more likely to be converter based. All battery storage needs a conversion from DC power to the AC grid [9]. Therefore, battery storage installations also act as CBDG units for the grid. They can replace a part of the conventional generation when they supply power to the grid.

Finally, there are more and more High Voltage Direct Current (HVDC)

connections in the power system [15]. These connections can connect generation to the system (e.g. an offshore Wind Power Plant (WPP) with many WTs) or they interconnect two regions of the AC system. In the first case, regardless of the type of generation that is connected through the system, this generation is converter based. In the second case, the HVDC connection will also act as a large CBDG unit. When other AC connections are removed from the system, this large CBDG unit replaces in fact conventional SGs.

In conclusion, it is clear that the share of CBDG units will increase. When the costs of power electronics decrease further, this trend will be reinforced by making battery storage and solar PV energy cheaper, by increasing the share of type 4 WTs and decreasing the share of other types of WTs, and by making HVDC connections in more cases an economic alternative to AC connections.

Converter Types

Until now, the power electronic interface has not been specified. Although there exist various alternative technologies, e.g. Current Source Converters (CSCs) and Voltage Source Converters (VSCs), most of the CBDG units, and several new HVDC connections, use a VSC [16, 17]. There are single-phase two-level VSCs that are used to connect very small CBDG units (e.g. smaller than 5 kVA in Belgium) in the Low Voltage (LV) grid. Larger CBDG units are connected through three-phase VSCs and there are several types: e.g. two-level, three-level, multilevel, ... This dissertation only considers these larger CBDG units that use three-phase three-leg VSCs.

In chapter 2, it will be shown that these CBDG units with a three-phase three-leg VSC can be controlled very fast and in chapter 3, this will be exploited to make simplified calculation models that are valid for all types of three-phase three-leg VSCs (two-level, three-level, multilevel, ...).

1.1.2 Problems with Increasing Share of Converter Based Distributed Generation

There are several problems described in literature when centralised generation with SGs is replaced by CBDG (or DG) units. When the classification is used from a report of EirGrid and SONI, the TSOs from Ireland and Northern Ireland, there can be issues related to [18][2]:

- *Frequency stability*

[2]The stability issues use the definitions provided in [19, 20].

- *Voltage stability*
- *Transient stability*
- *Voltage control*
- Network loading
- *Power balance fluctuations and frequency regulation*
- Small signal stability
- *Fault levels*

An extensive discussion of all these issues is out of scope of this work, but a selection of these issues, indicated in *italic*, is discussed below.

A large number of problems are related to the operation principles of the grid in (quasi) steady state due to the generation variability of many CBDG types. For instance, the control of the grid frequency is typically handled by large generators that can vary their active power output based on the grid frequency within a certain band. In addition, SGs can quite easily control their reactive power output within certain bands to help controlling the voltage in the grid. When CBDG units replace SGs in the system, there are fewer SGs in the system to control the frequency and voltage. In addition, the CBDG units (e.g. WTs, PV units, ...) often have a variable power output, leading to more power fluctuations. The combination of these effects, together with the change in grid inertia that is discussed next, makes the control of frequency and voltage a bigger challenge. (*Voltage control* and *Power balance fluctuations and frequency regulation*)

Other problems are related to handling incidents on the grid. All large SGs are coupled directly to the grid and their inertia contributes to the grid inertia: when there is an excess power in the grid, the SGs speed up, when there is a shortage of power, they slow down. This causes the grid frequency to change. The grid frequency has to be kept within a narrow band, as most generators and loads cannot handle too high or too low frequencies. They will be decoupled from the grid when the grid frequency deviation is too high, resulting in a possible loss of the functionality of the grid (a blackout). During incidents (e.g. when a generator disconnects from the system), the power balance in the grid can suddenly change and the grid frequency changes. When there is less inertia in the grid, the grid frequency changes faster and the decoupling of generators and loads from the grid happens more often and faster. As CBDG units are not connected directly to the grid, they don't contribute to the grid inertia. Much research on this problem and the creation of virtual inertia by CBDG

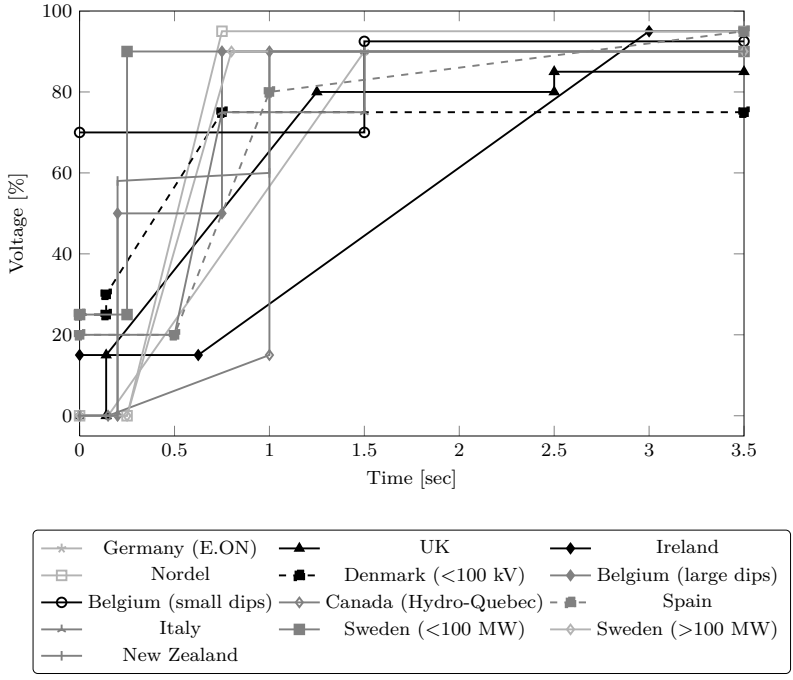


Figure 1.3: FRT requirements of various grid codes (source: [12, 23])

units has been performed (e.g. [12, 18, 21]) and this is not the focus of this work. (*Frequency stability*)

Another problem related to this, are the Fault Ride Through (FRT) requirements for generators. Whenever there is a considerable amount of DG units in the grid, it is important that they don't disconnect at the same time during an incident on the grid [22]. In the past, when the share of DG units was very limited, the disconnection of DG units didn't have a large impact on the grid frequency and the post-fault voltage. The centralised generation could also cover the power previously supplied by the DG units after an incident. When the share of DG units is high, a sudden, simultaneous disconnection of many DG units is problematic for the grid. Therefore, it is important that DG units don't disconnect for faults on the High Voltage (HV) grid. These faults are noticed in a widespread area, including on the lower voltage levels, but are typically cleared very quickly (e.g. <150 ms). Hence, FRT for low voltages is only required for short time durations. Figure 1.3 [12, 23] shows the FRT requirements for various grid codes for balanced faults. (*Frequency stability* and *Voltage stability*)

Finally, the problem that is the main focus of this dissertation is the effect of CBDG units, and the reducing number of SGs in the grid, on the fault currents and fault voltages in the grid. The next section explains the effect of power system faults in more detail. In summary, conventional SGs have a natural fault behaviour, that limits the impact of faults on the grid. On the other hand, CBDG units can control their fault behaviour. In addition, the fault currents of CBDG units are much lower than the fault currents of SGs. The main question is then how the CBDG units should be controlled to limit the impact of power system faults, when CBDG units replace a considerable amount of SGs in the power system. (*Transient stability* and *Fault levels*)

1.1.3 Power System Faults

Although the number of power system faults (or short-circuits) can be reduced with appropriate measures[3], it is not possible to eliminate all power system faults. Tall obstacles can hit overhead lines, excavators can hit underground cables, equipment can fail due to construction faults, ageing or overloading, lightning can hit installations, operational faults can occur, ...

There are several types of faults: series faults (in line with the system: e.g. broken conductor faults), shunt faults (a connection of the system with the ground or another part of the system: e.g. a single-line-to-ground fault) or a combination of both [24]. The effect of a fault depends on the type of fault, but in general, they should be isolated from the grid as fast as possible by the protection system to limit the impact of the fault on the loads and generation units.

In the remainder of this dissertation, only shunt faults are considered as they are the most common faults. Data from the UK [25] shows that for the HV grid 67% of these shunt faults are single-line-to-ground, 25% are line-to-line, 5% are three-phase and three-phase-to-ground and 3% are two-lines-to-ground faults.

Balanced Faults

Balanced or symmetrical faults are the same in all phases (i.e. symmetrical). Three-phase and three-phase-to-ground faults are balanced faults. In a balanced

[3]These appropriate measures include all aspects of the power system: power system design and construction (e.g. using reliable technologies, specifying appropriate equipment ratings, applying acceptance tests, ...), power system maintenance (e.g. timely maintenance, condition based maintenance through system monitoring, ...) and power system management (e.g. timely replacements, planning of civil works, ...).

power system, the ground connection plays no role as the sum of the line-to-ground voltages of the three phases is zero. Therefore, usually only three-phase faults are considered when balanced faults are discussed.

Although the three-phase faults are not the most common faults, they have the largest impact on the voltage in the system: an ideal three-phase fault is characterised by low voltages around the fault and, because of the network design, three-phase faults usually have the highest fault currents. They have the largest impact on the transient stability and the frequency of the system. A measure used to characterise the strength of the grid, and the amplitude of the short-circuit currents, is the short-circuit power S_{sc}:

$$S_{\mathrm{sc}} = \sqrt{3} \cdot U_{\mathrm{nom,LL}} \cdot I_{\mathrm{sc},3\varphi} \tag{1.1}$$

with $U_{\mathrm{nom,LL}}$ the nominal line-to-line voltage and $I_{\mathrm{sc},3\varphi}$ the three-phase short-circuit current at a point in the system. This is a fictive quantity that links quantities that do not occur simultaneously [26]. A high short-circuit power is positive for the detection of faults, for the transient stability of the system and for limiting the impact of the fault (a more local effect with a larger potential gradient). However, the short-circuit power cannot be too high [26]. On the one hand, the short-circuit withstand capability of the power system components determines which short-circuit current, during a certain time, causes permanent damage to the components due to mechanical forces or heat dissipation. On the other hand, the breaking capacity of the circuit breakers determines which short-circuit current can be interrupted by the circuit breakers. Exceeding this breaking capacity means the interruption of the fault is no longer guaranteed. This can lead to uncontrolled situations and very high damage to the system.

Conventional SGs inject large reactive currents into balanced faults and thus contribute to the short-circuit power of the grid. When they are replaced by CBDG units, the short-circuit power is expected to drop as there are fewer SGs in the system and the CBDG units have a limited overload capability. The question remains whether the fault response of CBDG units can influence the short-circuit power of the grid.

Unbalanced Faults

Unbalanced or asymmetrical faults are all other faults, e.g. line-to-line or single-line-to-ground faults. For these faults, the fault currents are typically lower and the residual voltage is higher. Unbalanced faults cause voltage unbalances in the three-phase power system (i.e. the voltage amplitudes of the three phases are not equal or the angle between the phases is not 120°). These voltage unbalances have adverse effects on all rotating machines in the grid (IGs, SGs)

as they cause torque fluctuations and excessive heating [27, 28]. Smaller voltage unbalances are also caused by unbalanced loading of the power system (e.g. single-phase connected loads).

Unbalanced faults are often described in symmetrical components. The fault analysis of positive, negative and zero sequence voltages and currents is historical. In addition, it is more intuitive than the fault analysis of the three-phase coupled network. The definitions of symmetrical components are given in appendix A.2. Other, more industrially focused, descriptions of fault types exist as well. The most used method is the description introduced by Math Bollen [29–31], where the resulting voltage sags of unbalanced faults, over transformers with different vector groups, are characterised with letters. In this dissertation, the description in symmetrical components is used as it is more general.

Conventional SGs inject positive and negative sequence currents into unbalanced faults [32]. These current injections increase the positive sequence voltage and decrease the negative sequence voltage in the grid. This way they naturally counteract the voltage unbalance. When they are replaced by CBDG units, the question is twofold: what is the effect of fewer SGs in the system and what is the effect of the CBDG units on the voltage unbalances and fault currents.

Power System Protection

The power system has to be protected to limit the impact of faults. Three aspects determine the protection system: protection of the equipment for excessive damage (due to the high currents or torque fluctuations), protection of the power system continuity (low voltages, frequency deviations, ... and resulting loss of loads) and protection for safety of the people (fire, mechanical forces, electrocution hazard, ...).

There are several types of protection systems (e.g. overcurrent relays, distance relays, differential relays, fuses, ... [33–35]). Most of the relays use local measurements of voltage, current, phase angle, frequency, ... to decide whether a circuit breaker should be triggered to isolate the faulted network part from the system. The goal is to do this as fast as possible[4], but also to obtain selectivity. Selectivity means that only the faulted network part is disconnected and no healthy parts are disconnected. For the distribution system, the protection system mainly consists of relays and fuses that are triggered based on the amplitude of the current [33,36,37]. Therefore, the fault levels at the distribution system are important. At the HV grid, often more advanced relays are used and therefore, the absolute fault level is less important from a protection system

[4]Typical fault clearing times range from less than 100 ms for HV grids to several hundreds of ms for certain faults at lower voltage levels [36].

point of view. However, it remains important as it limits the impact of the fault as discussed above.

1.2 Objectives and Scope Limitation

1.2.1 Objectives

The analysis of larger networks, with a great number of CBDG units, requires simple calculation models. This dissertation investigates which methods are suitable for evaluating the fault behaviour of CBDG units. A simplified method is selected, its assumptions are analysed theoretically and the method is validated. This method is capable of showing general trends of various fault current contribution strategies of CBDG units during balanced and unbalanced faults.

The controllability of CBDG units during faults is demonstrated to show that the fault behaviour of CBDG units is a design parameter. In literature and in standards, several strategies for the fault behaviour of CBDG units have been suggested. This work identifies the alternative strategies and their (dis)advantages.

Concerning balanced faults, much work has already been described in literature. Nevertheless, there are discussions among researchers on the short-circuit power trends. Based on the simplified calculation model, this work investigates the influence of the voltage support settings of CBDG units on the short-circuit power in the grid.

Concerning unbalanced faults, the general approach is to let CBDG units block negative sequence currents. This dissertation evaluates whether this is a good approach during unbalanced faults. Several alternative negative sequence current contribution strategies are compared and the general trends of these design choices are demonstrated. The advantages of the alternative strategies are discussed in scenarios with a high share of CBDG.

1.2.2 Scope Limitation

In this dissertation, only CBDG units are considered. As is clear from section 1.1.1, the share of CBDG is expected to increase in the future. However, a considerable amount of currently installed DG units uses a SG and a direct grid connection, e.g. CHP units. For these units, there are well established calculation models available and therefore, the focus is not on these units. For an important kind of DG units, the WTs, section 1.1.1 mentioned that the

most used WT type, type 3, uses a DFIG. How the share of type 3 and type 4 WTs will change in the future depends on numerous factors, but probably both types will be used in the near future. However, there is much research available on DFIG WTs and the choice was made not to treat this type of DG in this dissertation. Where appropriate, differences between DFIGs and CBDG units will be highlighted by referring to the appropriate research. Some dissertations that treat DFIGs in detail are mentioned here already: [38–40].

The control of CBDG units is an important factor in their fault behaviour. Although several control aspects are treated in this dissertation, the control of CBDG units is not the main focus of this dissertation. During this dissertation, a collaboration with Tobias Neumann, University of Duisburg-Essen, was set up. This resulted in several common publications. His dissertation will treat the control systems of CBDG units in much more detail.

To study the fault behaviour of CBDG units, the choice was made to develop a simplified model. This model focuses on the fundamental frequency fault behaviour and does not model any harmonic current injections by CBDG units during faults. Although some papers [41–43] have suggested injecting harmonic currents during unbalanced faults, these strategies are developed from a CBDG unit point of view and are most likely unacceptable for the grid when they are applied on a large scale. More recent publications from the same authors [44,45] also focus on the sinusoidal current injections during unbalanced faults. For these reasons, these harmonic strategies will not be evaluated in this dissertation.

As mentioned in section 1.1.1, this dissertation only considers the larger three-phase CBDG units. In addition, this dissertation only studies faults with a ground connection when there is a transformer, with a vector group that blocks the zero sequence currents, between the fault and the VSC of the CBDG unit. Most larger CBDG units have such a step-up transformer. This assumption avoids a detailed study on the earthing systems of the VSCs of CBDG units.

1.3 Outline of the Dissertation

Chapter 2 describes the control of CBDG units during balanced and unbalanced faults. It is shown that several control systems are developed in literature to control both the positive and negative sequence currents during faults. An elaborated case, based on a publication at the IEEE PES General Meeting in 2013 [46], illustrates that the fault behaviour of CBDG units is a design parameter. Several control aspects of the negative sequence current injection are discussed based on a publication made at the IEEE PES General Meeting of 2014 [47].

Chapter 3 describes several simulation and simplified calculation techniques developed in literature. ElectroMagnetic Transient (EMT) simulations with Averaged Value Models (AVMs) are selected to study the detailed behaviour of the control systems of CBDG units. Based on a paper presented at the IEEE PEDG conference in 2012 [48], their accuracy and the gain in simulation speed are evaluated through a comparison with EMT simulations that use switched models. Afterwards, an Iterative Linear Network Equations Method (ILNEM) is fine-tuned as this is the simplest method capable of modelling the fundamental frequency fault behaviour of (the control system of) CBDG units. The method is validated with detailed simulations to show its merits and its limitations.

Chapter 4 discusses the fault behaviour of CBDG units during *balanced* faults. As this is a well developed field, the literature shows interesting approaches. E.g. the effect of voltage support settings on the transient stability, the maximal current injection, the effect of the phase angle of the current injection, etc. ... are described in literature. During discussions with other researchers, the question arose whether CBDG units can contribute to the short-circuit power in the grid. A study described in a paper presented at the IEEE PowerTech conference of 2015 [49] illustrates this and this study is elaborated here.

Chapter 5 discusses the fault behaviour of CBDG units during *unbalanced* faults. During this PhD research, several discussions arose about the requirements for negative sequence current injection. The technical feasibility is illustrated in chapter 2, but standards imposing this were still in development. In addition, from a control point of view, other negative sequence current injections are considered in literature. The different approaches, including both blocking and injecting negative sequence currents, are compared and the conclusions from paper [50], to appear in IEEE Transactions on Energy Conversion, are summarised. The calculation framework developed in chapter 3 is used to illustrate the advantages of negative sequence current injection with case studies.

Chapter 6 summarises the general conclusions of this work and gives an outlook on further steps to be made within this field.

Chapter 2

Control of Converter Based Distributed Generation

"We can't control the wind, but
we can adjust the sails."
— Thomas S. Monson

2.1 Introduction

This chapter describes the control of Converter Based Distributed Generation (CBDG) units during symmetrical and asymmetrical faults. As the control of CBDG units is a well researched topic [16, 17], it is not the main focus of this dissertation. It is however seen as a required introduction to understand the fault behaviour of CBDG units. Therefore, section 2.2 gives a control overview of a CBDG unit during faults. References to several alternative control options in literature are given, where much deeper discussions of the control systems are described. Afterwards, examples of a flexible CBDG fault response, based on publication [46], presented at the IEEE PES General Meeting in 2013, are shown in section 2.3. These examples illustrate the main idea of this chapter: i.e. that the fault response of CBDG units is a design parameter. Finally, specific control aspects of negative sequence current injection are stressed in section 2.4. This part is based on publication [47], presented at the IEEE PES General Meeting in 2014.

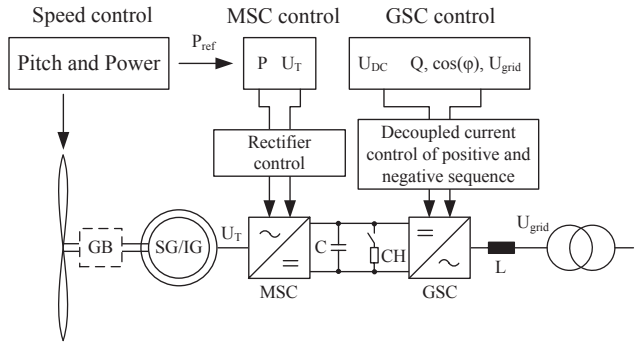


Figure 2.1: Overview of a CBDG unit: a WT unit
(C: capacitor, CH: chopper, GB: gearbox, L: inductor)

2.2 Control Overview of CBDG Units during Faults

This section describes the current controllers of CBDG units during symmetrical and asymmetrical faults. First, the general structure of a CBDG unit is given to explain the focus on the current controller during faults. Afterwards, the most intuitive current controller capable of controlling both the positive and negative sequence currents is discussed: the Double Synchronous Reference Frame (DSRF) current controller. At the end, references to alternative implementations of current controllers are listed.

2.2.1 Structure of CBDG Units

There is a common structure of CBDG units. The two main types of CBDG, a WT and a PV unit, are given in Figure 2.1 and 2.2. The primary side is different, but in both cases a primary power source is converted to DC power, either through a rectifier, the Machine Side Converter (MSC), or through a DC-DC converter. Afterwards, all CBDG units have a DC bus and then a DC to AC power electronic interface: the Grid Side Converter (GSC). As indicated in section 1.1.1, this GSC is a three-leg VSC for most CBDG units, except for the very small single-phase units that are not considered in this dissertation. There are different controllers for the DC bus voltage for different types of CBDG units [17]. In general during faults, the primary source power input is larger than the active power supplied to the grid. Therefore, the DC bus voltage will increase. Because of the FRT requirements, this DC bus voltage has to be limited in some way: either by a chopper or by acting on the primary source

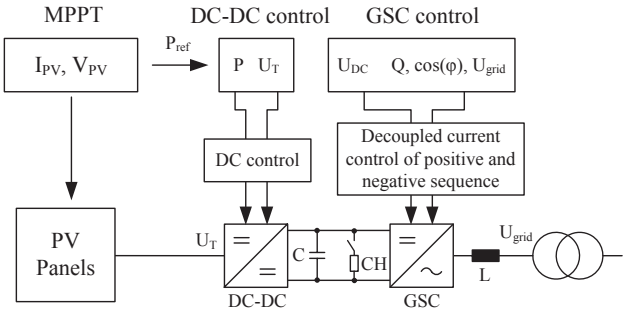


Figure 2.2: Overview of a CBDG unit: a PV unit (MPPT: Maximum Power Point Tracking)

(or a combination of both). Hence, the DC bus voltage will be more or less under control during the fault and for studying the grid impact of CBDG units during faults, mainly the response of the GSC is important. This GSC converts the DC bus power to AC power and the next section focuses on its control by assuming a constant DC bus voltage. This reasoning and the assumption of a constant DC bus voltage is also used in [51].

In the next section, it is shown that the positive and negative sequence currents can be controlled separately. The current control results in a certain voltage that has to be generated by the GSC, as the converter is a VSC. This means the current control system is more or less independent from the converter technology, but there is a step in between the voltage references and the control of the switches of the VSC (e.g. Space Vector Modulation (SVM) for a two-level VSC [52]).

2.2.2 Grid Side Converter Current Control from the DC Bus to the AC Grid

As was explained in section 1.1.3 of the introduction, power system faults have a short duration as they are isolated from the system as fast as possible. For induction or synchronous machines, the natural behaviour of the machine mainly determines the fault response. For CBDG units, the GSC determines the fault behaviour, as will be illustrated in section 2.3. Therefore, this section describes the control of the GSC current controller. Several alternative controllers exist, but this section describes a control in the synchronously rotating reference frame. This control system is the most intuitive as the controlled currents and voltages are all DC quantities [17].

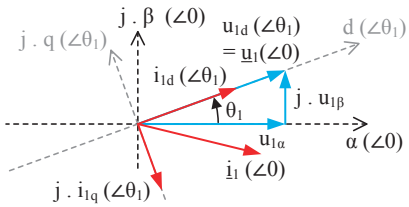


Figure 2.3: Voltage oriented reference frame in the positive sequence

Synchronous Reference Frame

The most simple control system is the Synchronous Reference Frame (SRF) control system (or control in the dq-frame[1]). It is a well-known control method [16, 17, 52]. In the AC grid, all signals are fundamental frequency AC signals during normal operation. Therefore, if all signals are expressed in a voltage oriented rotating reference frame, they become DC signals with a component along the direct (d) axis and along the quadrature (q) axis. This decomposition is illustrated for positive sequence signals in Figure 2.3. The $\angle$ symbol indicates the reference frame, where $\angle 0$ represents the fixed reference frame and $\angle\theta_1$ the reference frame aligned to the rotating positive sequence grid voltage (dq-frame).

When only DC signals have to be controlled, simple Proportional Integral (PI) controllers can be used [17, 52]. The grid current is controlled by equation (2.1a), assuming a simple inductor between the converter and the measurement of the grid voltage. These equations are expressed in dq coordinates in (2.1b)-(2.1c). This results in the control system shown in Figure 2.4: a certain reference voltage (u_{ref}) is generated by the converter to control the current through the inductor [17].

$$u_{\text{ref}} - u_{\text{grid}} = R \cdot i + L \cdot \frac{di}{dt} \tag{2.1a}$$

$$u_{d,\text{ref}} - u_{d,\text{grid}} = R \cdot i_d + L \cdot \left(\frac{di_d}{dt} - \omega \cdot i_q \right) \tag{2.1b}$$

$$u_{q,\text{ref}} - u_{q,\text{grid}} = R \cdot i_q + L \cdot \left(\frac{di_q}{dt} + \omega \cdot i_d \right) \tag{2.1c}$$

[1]The nomenclature from [17] is used here. This control system uses a voltage oriented control, i.e. the reference frame is oriented to the grid voltage. During transients, this reference frame does not rotate at synchronous speed.

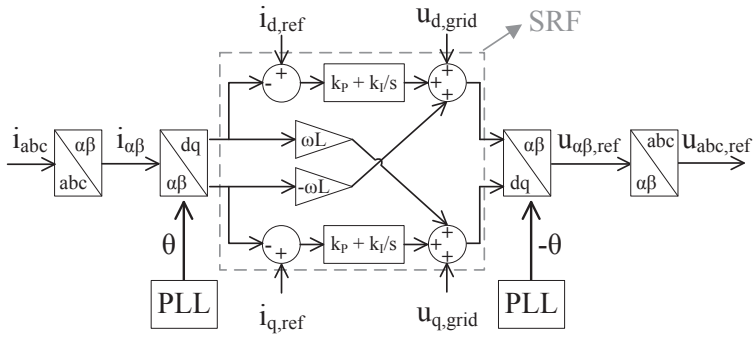


Figure 2.4: Synchronous Reference Frame control system

Two transformations are given in this scheme: the Clarke ($abc \rightarrow \alpha\beta$), see (2.2), and the Park transformation ($\alpha\beta \rightarrow dq$), see (2.3). The Clarke transformation transforms the three-phase signal to a two-phase signal as there is no zero sequence current component in a three-leg converter.

$$u_\alpha = \frac{2}{3} \cdot \left(u_a - \frac{1}{2}\, u_b - \frac{1}{2}\, u_c \right) \tag{2.2a}$$

$$u_\beta = \frac{1}{\sqrt{3}} \cdot (u_b - u_c) \tag{2.2b}$$

$$u_0 = \frac{1}{3} \cdot (u_a + u_b + u_c) \tag{2.2c}$$

Note that this transformation is not power invariant [52]. An alternative power invariant transformation exists, but the basic idea for the control system is the same: the three abc values are transformed to $\alpha\beta$ values.

The Park transformation transforms the $\alpha\beta$ signals to a rotating reference frame with the angle of rotation θ:

$$u_d + j \cdot u_q = e^{-j \cdot \theta} \cdot (u_\alpha + j \cdot u_\beta) \tag{2.3a}$$

$$u_d = \cos\theta \cdot u_\alpha + \sin\theta \cdot u_\beta \tag{2.3b}$$

$$u_q = -\sin\theta \cdot u_\alpha + \cos\theta \cdot u_\beta \tag{2.3c}$$

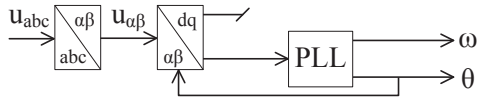


Figure 2.5: Simple Phase Locked Loop

In this scheme the angle estimation θ is done by the Phase Locked Loop (PLL). Especially during voltage unbalances or harmonics, the design of the PLL is crucial for a good performance of the controller [17, 53, 54]. The next section discusses the PLL in more detail.

Phase Locked Loop

A Phase Locked Loop (PLL) estimates the phase angle of the grid voltage. In general, a PLL is used to drive the q component of the measured grid voltage to zero with a PI controller. The general principle is shown in Figure 2.5.

During fault situations, positive, negative and zero sequence voltages appear. Using standard PLL structures results in a bad estimation of the positive sequence angle [55] and a degraded performance of the whole control system under unbalanced voltages. Several methods to separate positive and negative sequence fundamental frequency components have been developed and are described in literature [17, 48, 53, 54, 56]. After this separation, the positive sequence angle is determined from the positive sequence voltage with a standard PLL. The negative sequence angle (or the angle of the complex conjugate negative sequence voltage) can be estimated with a second PLL.

As explained in appendix A, the total space vector is the sum of the positive sequence (rotating counter-clockwise) and the complex conjugate of the negative sequence space vector (rotating clockwise). In section 2.4, the negative sequence phase angle estimation will be discussed in further detail, but it is clear that the angle of the fundamental frequency negative sequence voltage, θ_2, is related to the angle of the fundamental frequency positive sequence voltage, θ_1, by equation (2.4), where γ is constant in steady state. The angle of the complex conjugate negative sequence voltage, represented by θ_2^* in this dissertation, is of course the opposite of θ_2.

$$\theta_2^* = -\theta_2 = -\theta_1 + \gamma \tag{2.4}$$

The zero sequence angle is usually not required, but can be determined with an additional PLL after using (2.2c) to determine the zero sequence voltage.

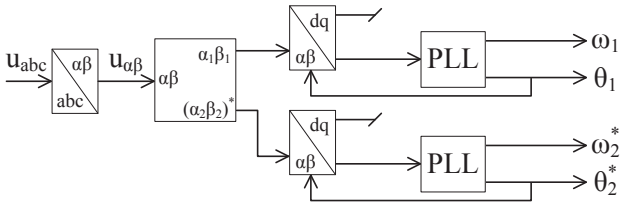


Figure 2.6: Phase Locked Loop with positive / negative sequence separation

The main idea of the different positive-negative sequence separation methods is to apply a filter to obtain the fundamental frequency components and a 90° phase shifted signal. Afterwards, the instantaneous symmetrical components transformation, as described in [57], can be applied. These methods differ in speed (with respect to changes) and in robustness (with respect to harmonic distortion). In this work, the separation of positive and negative sequence components is made after the Clarke transformation ($abc \rightarrow \alpha\beta$), see Figure 2.6, similar to [56]. Although more advanced filtering techniques have a better performance with distorted voltage signals, this delayed signal method was chosen for its simplicity. In [39], a much faster positive-negative sequence separation, the Lê method [58], and a more robust modification to this method are described. A good overview of several other PLL implementations can be found in [17]. For the remainder of this work, it is sufficient to know that both the positive and negative sequence angle can be estimated with a PLL.

Double Synchronous Reference Frame

The biggest limitation of the SRF control scheme is that only the positive sequence current is controlled and the negative sequence current is uncontrolled. Therefore, a Double Synchronous Reference Frame (DSRF) control scheme was developed [59]. This controller is capable of controlling a VSC's positive and negative sequence current. In Figure 2.7, the general structure of a DSRF current controller is shown. First, a Clarke ($abc \rightarrow \alpha\beta$) transformation is applied. Afterwards, two voltage oriented reference frames are made by transforming these currents to the positive sequence voltage oriented reference frame (with angle θ_1, see Figure 2.3) and to the complex conjugate negative sequence voltage oriented reference frame (with angle θ_2^*, see Figure 2.8). This means that the total current is transformed to both reference frames. Therefore, there is a DC[2] component, the positive sequence current, and a second harmonic

[2]In steady state, this is a DC component, but in dynamic situations, this will be a slowly changing component.

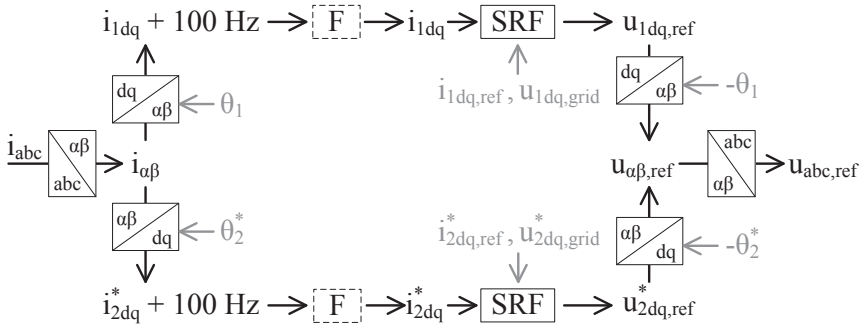


Figure 2.7: Double Synchronous Reference Frame control system

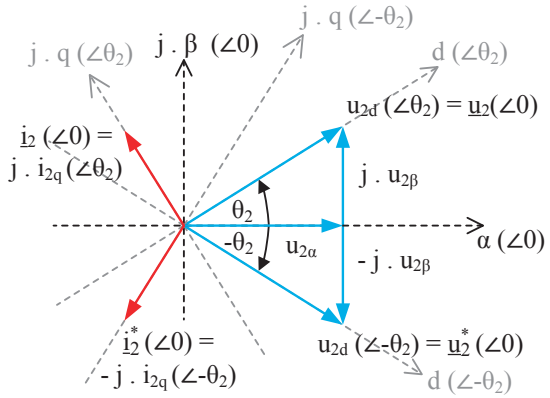


Figure 2.8: Voltage oriented reference frame in the (complex conjugate) negative sequence

component (100 Hz for a nominal grid frequency of 50 Hz) in the positive sequence reference frame. Likewise, the negative sequence frame contains a DC component, the negative sequence current, and a second harmonic component. By removing the second harmonic components with a band stop filter (see Figure 2.7: "F"), a classic DC control system can be built to control the positive and negative sequence currents towards their setpoints $i_{1dq,\mathrm{ref}}$ and $i_{2dq,\mathrm{ref}}$ (see Figure 2.7: "SRF", similar to the "SRF" indicated in Figure 2.4). This means that simple PI controllers can be used to avoid steady state errors. The reference signal for the converter, $u_{abc,\mathrm{ref}}$, is calculated by transforming the positive and negative sequence reference frames back to the stationary frame, adding both and applying the inverse Clarke transformation (see Figure 2.7).

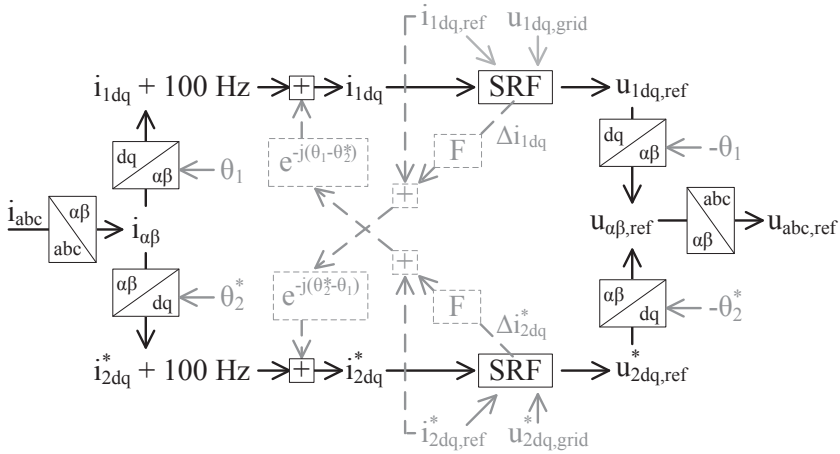


Figure 2.9: Decoupled Double Synchronous Reference Frame control system

However, the band stop filters, that were used in [59] to suppress the positive sequence components in the negative sequence frame and vice versa, lead to phase delays and instability of the controller when a fast current control is required [60]. This results in a relatively slow current control, unsuitable for the purposes of fault current control within a few fundamental periods ($\ll 100$ ms).

An improvement to the DSRF current controller scheme is described in [61]: the Decoupled Double Synchronous Reference Frame (DDSRF) current controller. This controller no longer uses band stop filters, but instead uses a decoupling system to remove the second harmonic components in the positive and negative sequence control frames. The principle is illustrated in Figure 2.9. The feedback filters for the error signals Δi_{1dq} and Δi_{2dq} in the decoupling loop (see Figure 2.9: "F"), can be tuned to obtain a fast current control. More details about the DDSRF scheme are found in [61].

Both the DSRF and the DDSRF schemes require a decent estimation of both the positive and the negative sequence angle with a PLL, as described above. In section 2.3, the performance of the DDSRF current controller is demonstrated.

2.2.3 Alternative Implementations

Several alternatives to the DDSRF current controller exist. Certain controllers have specific advantages: e.g. a less stringent phase angle estimation requirement because they control the CBDG unit in the fixed reference frame $\alpha\beta$ with

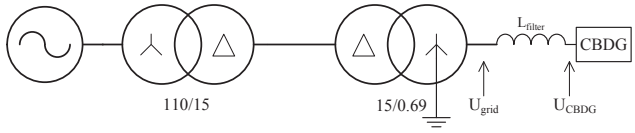


Figure 2.10: Grid model

Proportional Resonant (PR) controllers or an improved fault behaviour with deadbeat controllers [62]. For this work, the exact implementation of the controller is not important, but it is important to know that both the positive and negative sequence current can be controlled during asymmetrical faults. Therefore, section 2.3 illustrates the fault response of a CBDG unit during faults. More details about other control systems are found in literature. The books [16, 17] give a good overview of alternative controllers.

2.3 Example of Flexible CBDG Fault Current Response

In this section, an example of the flexible fault current contribution of a CBDG unit is given. This example was reported in publication [46] to illustrate that the fault response of CBDG units is determined by their control system. This way, their fault response becomes a design parameter. The CBDG unit uses the DDSRF current controller and the PLL described in section 2.2.2 to control the positive and negative sequence current separately. The simulation is made with the PSCAD software [63] and the converter is modelled as an Averaged Value Model (AVM). These AVMs will be discussed in more detail in chapter 3. For now, it is sufficient to know that an AVM is a simplified model where the switching actions of the power electronics are averaged and that this technique is validated in literature as a suitable technique to study the control systems of CBDG units [16, 48].

2.3.1 Simulation Model

Figure 2.10 shows the grid model that is used and Table 2.1 summarises the grid properties. The Medium Voltage (MV) voltage level was chosen to be 15 kV[3]. The CBDG unit is connected to 690 V. In the control system, the inverse of

[3]Any voltage around 10-20 kV is realistic for European MV distribution networks: e.g. the CIGRE benchmark grid for integrating DG in MV distribution networks is based on a

Table 2.1: Grid data

Element	Property	Value
HV grid	U_{nom}	110 kV
	S_{sc}	1200 MVA
	X/R ratio	10
	f_{nom}	50 Hz
MV transformer	S_{nom}	40 MVA
	U_{nom}	110 kV / 15 kV
	Vector group	Yd11
	u_k	12%
	u_r	0.5%
LV transformer	S_{nom}	2 MVA
	U_{nom}	15 kV / 690 V
	Vector group	Dy11 (solidly earthed)
	u_k	6%
	u_r	0.95%
CBDG unit	S_{nom}	2000 kVA
	$U_{nom,DC}$	2650 V (constant)
Filter	L	1 mH (1.32 p.u.)
	R	3 mΩ (0.013 p.u.)

the positive sequence phase angle is used for the complex conjugate negative sequence phase angle for situations without a negative sequence voltage. As this approach is not correct if the goal is to control the in-phase and quadrature negative sequence currents individually, the negative sequence phase angle is tracked by the PLL when there is a negative sequence voltage, as shown in Figure 2.6.

As an additional simplification, the DC bus voltage is kept constant. This allows evaluating the performance of the DDSRF current controller without considering the impact of the DC bus voltage in the simulations. This DC bus voltage is chosen relatively high because of three reasons:

German MV grid and has a voltage level of 20 kV [64], while other studies of European MV grids have lower voltage levels: 10 kV in the Netherlands [65] and 11 kV in the UK [66].

1. Sinusoidal Pulse Width Modulation (PWM) is used in the simulation model as opposed to the more efficient SVM
2. The filter has a (too) high inductance value
3. The CBDG unit is designed to be capable of delivering 100% reactive current at nominal voltage (see (2.5), with U_{CBDG} and U_{grid} as indicated in Figure 2.10 and U_{DC} the required DC bus voltage)

$$\begin{aligned} U_{\text{CBDG}} &= I_{\text{CBDG}} \cdot Z_{\text{filter}} + U_{\text{grid}} \\ &= 1674 \cdot e^{-j\frac{\pi}{2}} \cdot (0.0030 + j\,0.3142) + \frac{690}{\sqrt{3}} \\ \Rightarrow\ U_{\text{DC}} &= |U_{\text{CBDG}}| \cdot \sqrt{2} \cdot 2 = 2614\,\text{V} \end{aligned} \tag{2.5}$$

The magnitude of the DC bus voltage determines how much current can be injected without overmodulation. This is discussed further in section 2.4.3 and in chapter 5, section 5.2.1. In this section, the high DC bus voltage allows injecting high currents without overmodulation.

2.3.2 Fault Cases

In all simulations, the CBDG unit delivers half of its rated current with a power factor equal to 0.95 before the fault (P = 0.95 MW, Q = 0.31 MVAr (capacitive)). Then, line-to-line faults and three-phase faults are applied to the LV and MV side of the step-up transformer at $t = 5\,\text{s}$. The faults are always removed at $t = 5.2\,\text{s}$.

In this section and throughout this dissertation, the results of CBDG units are given in the generator sign convention, as explained in appendix A.1. The opposite of the quadrature positive sequence current, $-i_{1q}$, is shown instead of i_{1q} to obtain all positive components in the figures.

Line-to-Line Fault at LV Side

In the first simulation, an ideal ($R_{fault} \approx 0\,\Omega$) line-to-line fault between phase b and c is applied at the LV side of the step-up transformer. Only the filter impedance is between the fault and the CBDG unit.

To illustrate that the CBDG unit can react in a random way, three different current setpoint strategies are applied. All strategies change the current

setpoints during the fault, based on the d component of the positive and negative sequence voltage, measured in their respective voltage oriented reference frames. These strategies are not realistic strategies. The goal of this section is only to illustrate that the current contribution of the CBDG unit is determined by the current setpoints during the fault. Realistic current contribution strategies during unbalanced faults are discussed in chapter 5.

In strategy A (Figure 2.11), only positive sequence currents are injected (the maximal reactive current). Figure 2.11a-2.11b show the grid voltages at LV and MV before and during the fault. Figure 2.11c shows the voltages as measured by the PLL (positive and negative sequence voltage are equal at the location of the fault) and Figure 2.11d gives the setpoints of the current controller before, during and after the fault. Figure 2.11e then gives the output current of the CBDG unit. As can be seen, both the settling time at the start ($t = 5\,\mathrm{s}$) and at the end ($t = 5.2\,\mathrm{s}$) of the fault are very fast. The d-components of the voltage measurements in the voltage oriented reference frames have a fast settling time, but exhibit some transients.

In strategy B (Figure 2.12), other setpoints are chosen during the fault: the negative sequence quadrature current i_{2q} is related to the negative sequence voltage u_{2d} according to (2.6) and the positive sequence in-phase current i_{1d} is reduced during faults.

$$i_{2q} = -\frac{u_{2d}}{u_{1d}} \cdot i_{1q} \tag{2.6}$$

In strategy C (Figure 2.13), the current setpoints are unaltered during the fault. For both strategy B and C, the voltage during the fault is not shown as it is very similar to strategy A. This is due to the limited short-circuit power of the CBDG unit compared to the grid.

The fault current responses and the setpoints that are applied (see Figure 2.12 and Figure 2.13) illustrate that a totally different fault current response, with a fast settling time, is obtained by applying different setpoints. This means that the fault behaviour of CBDG units can be changed in a flexible way according to the grid requirements.

Line-to-Line Fault at MV Side

In the next simulation, an ideal ($\mathrm{R_{fault}} \approx 0\,\Omega$) line-to-line fault between phase b and c is applied at the MV side of the step-up transformer. The same setpoint strategies A and B are used here and the results are given in Figure 2.14 (strategy A) and Figure 2.15 (strategy B). Again it is shown that just by

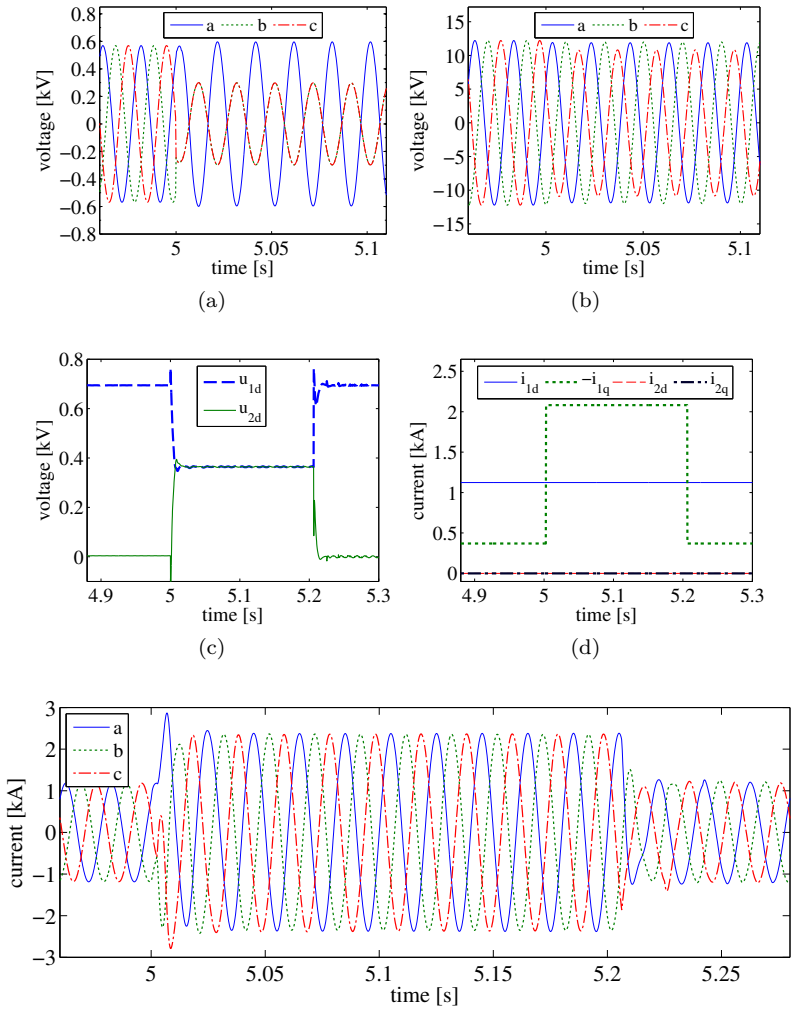
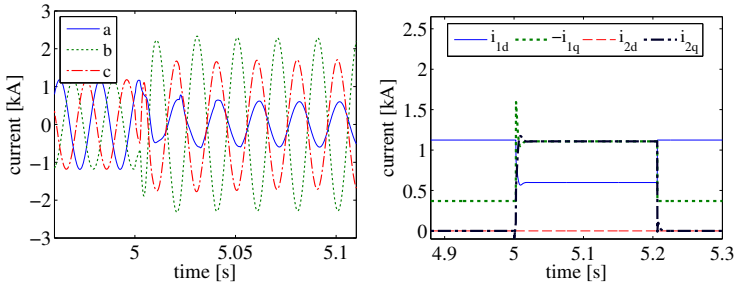
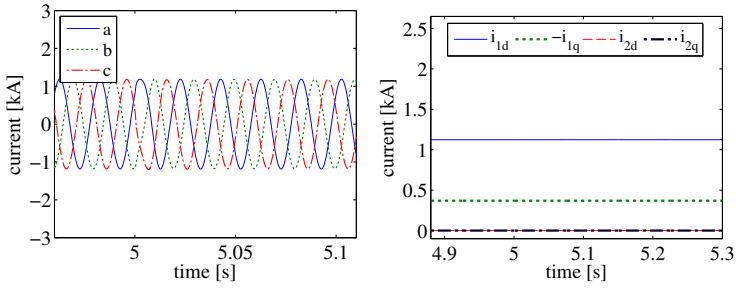


Figure 2.11: Line-to-line fault at LV, strategy A (no negative sequence current injection): (a) Voltage at the LV side and (b) at the MV side of the step-up transformer. (c) Positive and negative sequence voltage as measured by the PLL. (d) Setpoints (in the voltage oriented reference frames) of all sequence components. (e) CBDG output current at LV (before the step-up transformer).



(a) (b)

Figure 2.12: Line-to-line fault at LV, strategy B (with negative sequence current injection): (a) CBDG output current at LV. (b) Setpoints (in the voltage oriented reference frames) of all sequence components.



(a) (b)

Figure 2.13: Line-to-line fault at LV, strategy C (no change in current setpoints): (a) CBDG output current at LV. (b) Setpoints (in the voltage oriented reference frames) of all sequence components.

applying a different setpoint strategy during the fault, a totally different fault response is obtained.

Three-Phase Fault at LV Side

In case of a three-phase fault at the LV side of the step-up transformer, the voltage at the CBDG unit is about zero. The PLL is then unable to track the phase angles. Because most faults at the LV side of the step-up transformer are permanent, these faults will usually require a disconnection of the CBDG

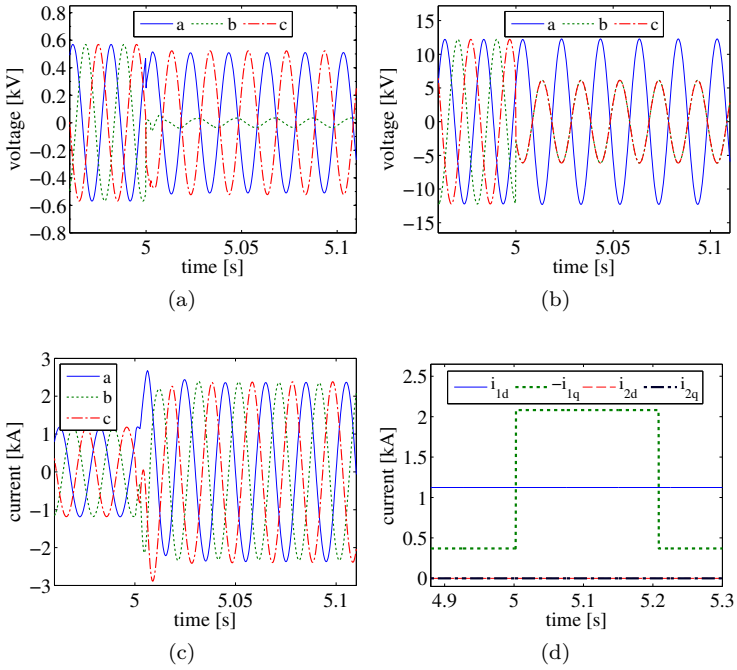


Figure 2.14: Line-to-line fault at MV, strategy A (no negative sequence current injection): (a) Voltage at the LV side and (b) at the MV side of the step-up transformer. (c) CBDG output current at LV. (d) Setpoints (in the voltage oriented reference frames) of all sequence components.

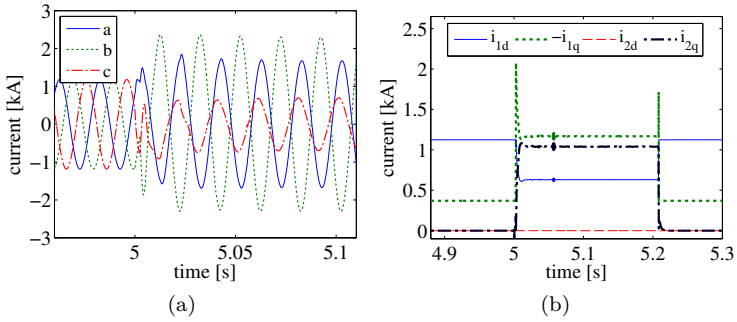


Figure 2.15: Line-to-line fault at MV, strategy B (with negative sequence current injection): (a) CBDG output current at LV. (b) Setpoints (in the voltage oriented reference frames) of all sequence components.

unit from the grid. In other cases, the converter of the CBDG unit should be blocked and kept off-line to restart as soon as the voltage is normalised again.

Three-Phase Fault at MV Side

Next, a three-phase fault is applied at the MV level ($R_{fault} = 0.5\,\Omega$). In this fault case, there is no negative sequence voltage. Two different strategies are shown. Strategy A (Figure 2.16) is the same as in the previous cases. In strategy D (Figure 2.17), the quadrature negative sequence current i_{2q} during a fault is set to be the opposite of the quadrature positive sequence current i_{1q}. Of course, this is not a realistic current contribution strategy during a balanced fault, but this strategy clearly illustrates that the fault behaviour of the CBDG unit is a design parameter.

In these simulations, the PLL settling time is a bit longer, which is noticeable in the injected currents of both Figure 2.16c and Figure 2.17a. The fault response of the latter (strategy D) is completely different from the former (strategy A), again demonstrating the flexibility of the control scheme.

2.4 Control Aspects of Negative Sequence Current Injection

This section describes the work that was done regarding control aspects of negative sequence current injection during this dissertation. It is based on publication [47], presented at the IEEE PES General Meeting in 2014, but some nuances on these results are made additionally.

First the negative sequence angle detection and the timing of the negative sequence current injection are discussed. Next, the related topic of the influence of the negative sequence current injection on the voltage recovery after the fault is treated. Finally, the voltage and current limitation of the CBDG during unbalanced voltages and negative sequence current injection are considered.

2.4.1 Negative Sequence Angle Detection and Timing of the Negative Sequence Current Injection

During unbalanced and also during balanced conditions in the power system, mathematical algorithms in the controller decompose the instantaneous values of voltage and currents in positive and negative sequence and control them

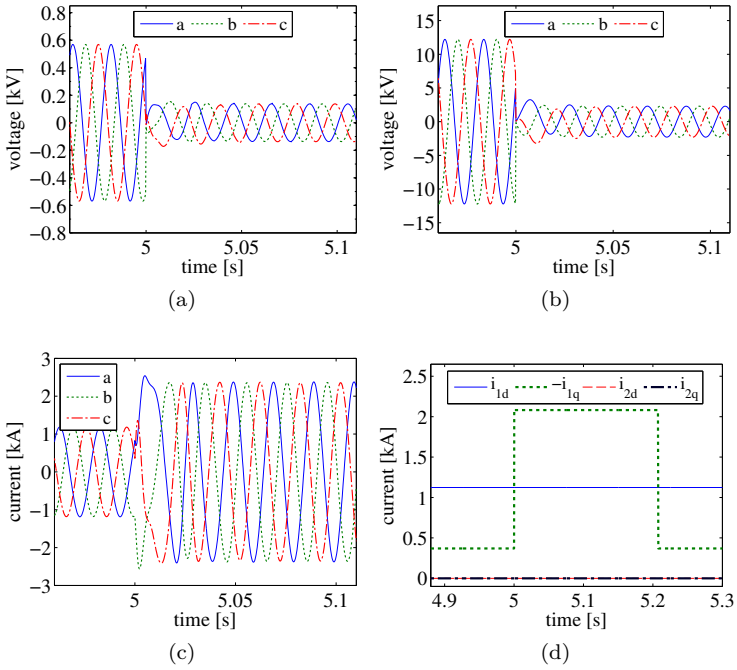


Figure 2.16: Three-phase fault at MV, strategy A (no negative sequence current injection): (a) Voltage at the LV side and (b) at the MV side of the step-up transformer. (c) CBDG output current at LV. (d) Setpoints (in the voltage oriented reference frames) of all sequence components.

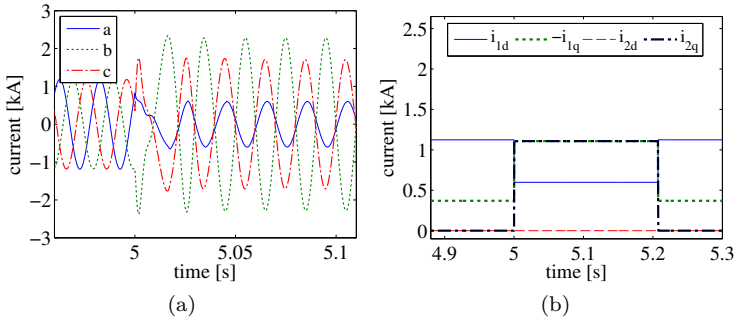


Figure 2.17: Three-phase fault at MV, strategy D (with negative sequence current injection): (a) CBDG output current at LV. (b) Setpoints (in the voltage oriented reference frames) of all sequence components.

separately and decoupled from each other (see section 2.2). After this separation, the phase angle of the negative sequence voltage can be calculated from its space vector (see Figure 2.8). In balanced conditions, without negative sequence in the system, the magnitude of the negative sequence voltage space vector is very small and disturbed by noise of the measurements. Input filters reduce the noise for an accurate utilisation of the signals in the control loops, but cannot avoid the noise totally. With a small magnitude of the negative sequence voltage space vector, the accurate phase angle calculation is problematic and sometimes even impossible.

As long as the control target of the negative sequence controller is zero negative sequence current, it is not required to align the negative sequence control loop to the negative sequence phase angle. Because the positive sequence angular speed is the same as the negative sequence angular speed, the positive sequence angle can be used as the reference angle for the Park transformation ($\alpha\beta \rightarrow dq$) in the negative sequence control loop during balanced conditions. This results in wrong dq components for the negative sequence current as the negative sequence phase angle is not the same as the positive sequence phase angle, see (2.4). However, when these dq components are both controlled to zero, the total negative sequence current is controlled to zero.

By contrast, for the dynamic injection of a certain negative sequence current during unbalanced fault conditions, detecting the phase angle of the negative sequence voltage must be performed fast and accurately in order to give the negative sequence current the correct alignment. This alignment is required for the voltage support to inject a negative sequence inductive reactive current, as will be explained in chapter 5. A wrong alignment can impact the situation in a negative way. During a fault, it is also important that the phase angle of the negative sequence angle is tracked continuously. Faults can evolve, e.g. from a single-line-to-ground to a two-lines-to-ground fault, and the phase angle of the negative sequence voltage then makes a phase jump. These evolving faults are not treated further in this dissertation.

In order to determine the phase angle of the negative sequence voltage accurately, a certain magnitude of the negative sequence voltage must exist. This leads to the implementation of a deadband for the dynamic negative sequence control. Figure 2.18 and 2.19 show simulation results for far away line-to-line grid faults which lead to a decrease in the positive sequence voltage and an increase of the negative sequence voltage. In the figures, the internally measured voltage signals of a simulated LV CBDG unit are visualised (for Figure 2.19 the positive sequence signals are omitted as they are similar to the ones in Figure 2.18). In the first example, the conjugate complex negative sequence space vector has a magnitude of 0.1 per unit (p.u.), which leads to an accurate calculation of the negative sequence phase angle. In the second example, the magnitude of the

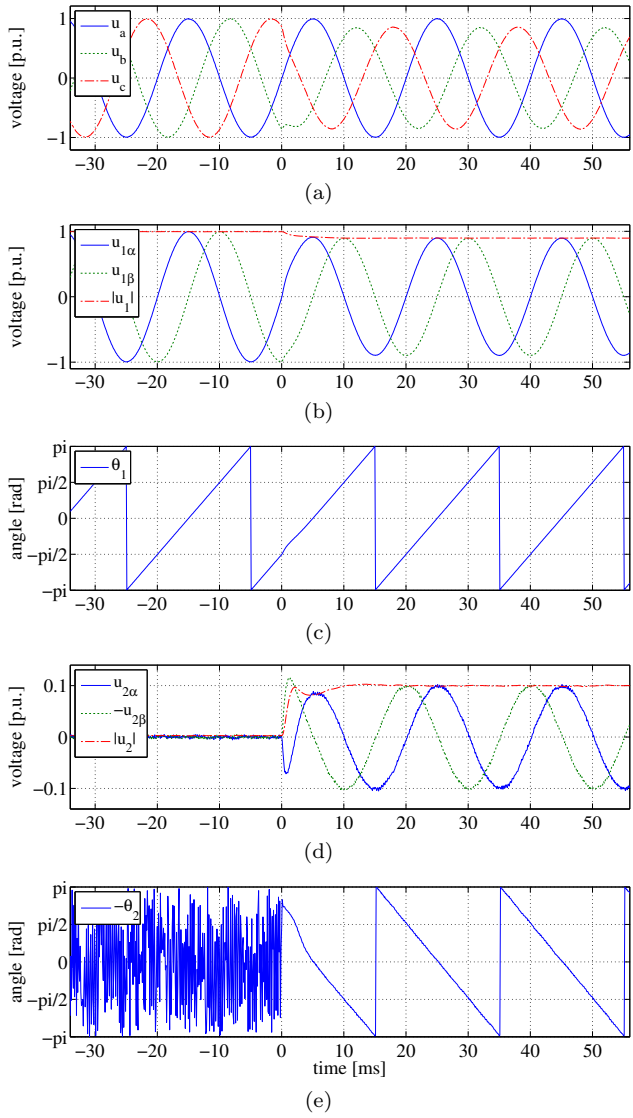


Figure 2.18: PLL angle estimation during 10% positive sequence voltage reduction and 10% negative sequence voltage increase at 0 ms: (a) Grid line-to-ground voltage, (b) positive sequence space vector, (c) positive sequence phase angle, (d) complex conjugate negative sequence space vector, (e) negative sequence phase angle.

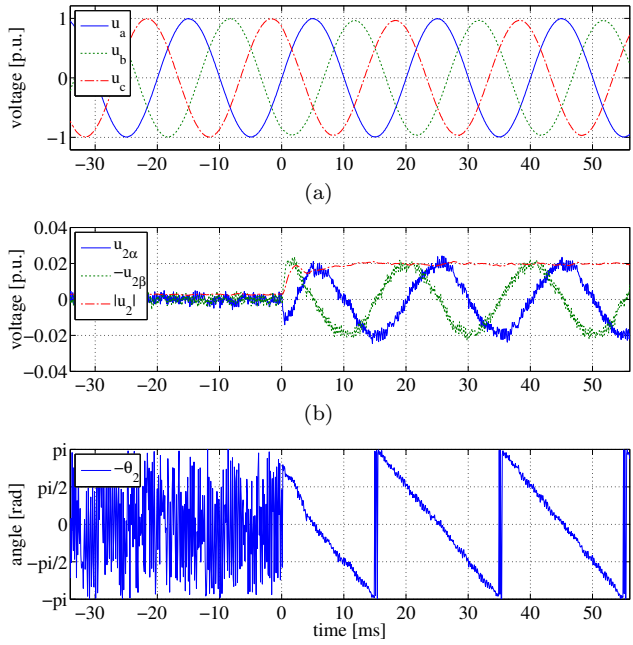


Figure 2.19: PLL angle estimation during 2% negative sequence voltage increase at 0 ms: (a) Grid line-to-ground voltage, (b) complex conjugate negative sequence space vector, (c) negative sequence phase angle.

negative sequence space vector is limited to 0.02 p.u.. As a result, the negative sequence angle calculation has undesirable noise on the signal which leads to an inaccurate control of the negative sequence current injection. A deadband of the negative sequence voltage of at least 0.05 p.u. seems to be a good compromise.

Additionally, Figure 2.18 illustrates another aspect: an accurate estimation of the negative sequence angle requires a quarter to half of a period (5-10 ms at 50 Hz) because the information in the sine wave is only fully known after that period of time.

The simulations described above use a similar control system as given in Figure 2.6 [67]: the phase angle is estimated based on the negative sequence voltage. It is however possible to use angular speed information from the positive sequence and only estimate the angle difference γ as defined in (2.4) by determining the angle of the complex conjugate negative sequence voltage according to the reference frame with angle $-\theta_1$ (determining the angle of

$\underline{u}_2^{*\angle -\theta_1}$). It is expected that this approach leads to a better estimation of θ_2 when the negative sequence voltage is low. This principle is not elaborated in this work as optimising the control systems is not the main focus of this work. In general, it can be concluded that the performance of the control system during low negative sequence voltages should be studied carefully and, when necessary, a small deadband might have to be applied for the control.

There are two specific cases when the angle θ_2 is not important and the angle θ_1 can be used: when the negative sequence current is blocked, the feed-forward voltage in the control loop (see Figure 2.9) makes sure there is no voltage difference in the negative sequence, so no negative sequence current will flow (neglecting measurement errors). The second case is when the CBDG only generates positive sequence voltages and forms an impedance in the negative sequence voltage. In this case no negative sequence voltages are generated and therefore no angle estimation of θ_2 is required. The importance of this last strategy will become clear in chapter 5.

2.4.2 Negative Sequence Current Injection Influence on Voltage Recovery after the Fault

An other aspect that needs to be considered for the dynamic negative sequence control is the effect of negative sequence current injection during voltage recovery. The transient period between the end of the fault and the stable post fault conditions seems to be critical with respect to the voltage quality because both negative and positive sequence reactive current injections for the voltage support in the corresponding sequence always have a small delay. As a consequence, the injected currents will influence the voltages that are measured by the CBDG unit and will complicate the fast estimation of the new positive and negative sequence voltages which can lead to inaccurate control actions. In addition, the mathematical algorithms for decomposing the instantaneous values into symmetrical components have a delay in the range of a quarter to half of a period (5-10 ms at 50 Hz) because the information in the sine wave is only fully known after that period of time, as was already mentioned in section 2.4.1.

To illustrate this effect of the negative sequence current injection on the voltage recovery, a simulation of a WPP with type 4 WTs is made. The simulation uses an aggregated single machine equivalent model. This aggregated model has a 70 MVA 690 V GSC (with a 1.4 p.u. short-term overload capability), a 84 MVA MV/LV transformer (u_k = 5%, vector group Dy) and a 91 MVA HV/MV transformer (u_k = 16%, vector group Yd). Figure 2.20 shows the response of the GSC of this aggregated model during a line-to-line fault at the 110 kV HV grid. During this fault, there is a reactive current injection in the positive sequence,

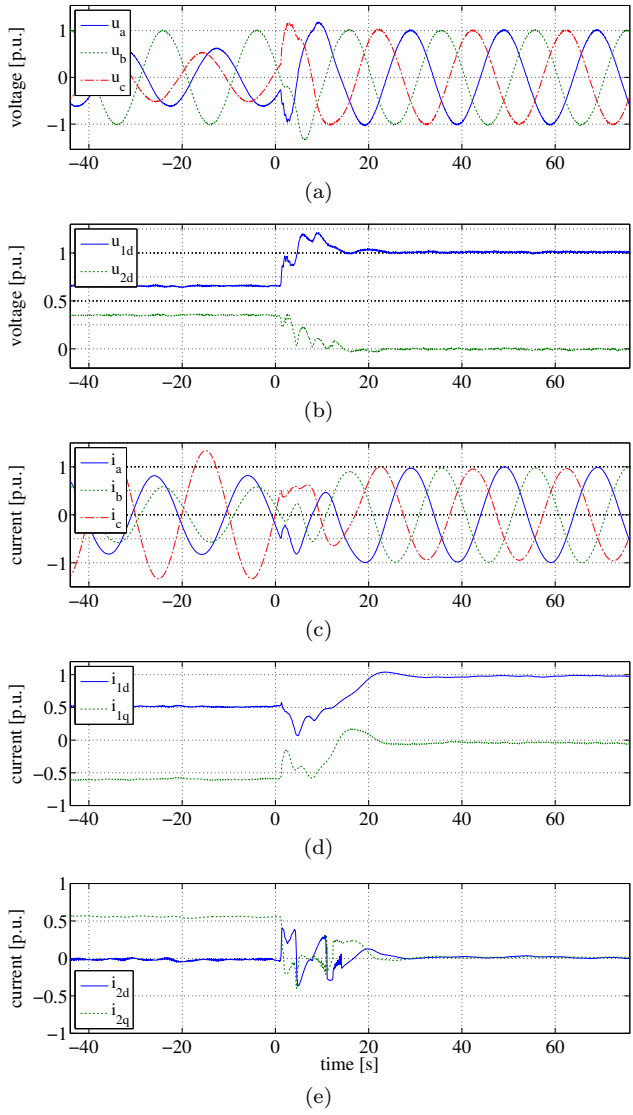


Figure 2.20: Voltages and currents during the voltage recovery of a WPP with type 4 WTs (end of fault at 0 ms): (a) Grid line-to-ground voltage, (b) positive and negative sequence voltage, (c) phase currents, (d) positive sequence current, (e) negative sequence current.

represented by i_{1q} (capacitive, i.e. negative in the generator sign convention), as well as in the negative sequence, represented by i_{2q} (inductive, i.e. positive in the generator sign convention), and the active current is reduced to keep the CBDG unit current within its limits (here 1.4 p.u.). (More information on the current limitation follows in section 2.4.3.) After fault clearing, both reactive currents are reduced to zero, while the active current in the positive sequence is ramped up to its prefault value of 1 p.u. The instantaneous values of voltages and currents show that the transient period of recovery takes roughly 10 ms. The shape of the voltage during this period is very fault-specific and depends on the grid topology and the connected generation units.

From a controller point of view, there is no reason to have a deadband in the positive sequence current controller as the positive sequence angle can be estimated accurately near the normal operating points of the CBDG unit. However, for the negative sequence current controller it is recommended to reduce the reactive current injection immediately after the negative sequence voltage is within the deadband required for the negative sequence angle estimation (see section 2.4.1). This reduces any adverse effects of the negative sequence current injection during voltage recovery and avoids problems with the alignment of the negative sequence current, as was discussed in section 2.4.1.

2.4.3 CBDG Current and Voltage Limitation

Influence of Negative Sequence Current Injection on the CBDG Current Limitation

For a CBDG unit, the total fault current contribution is limited by the converter rating. Injecting negative sequence current in addition to positive sequence current limits the amount of positive sequence current that can be injected. A straightforward limitation of the positive and negative sequence current can be applied [67]:

$$|\underline{i}_1| + |\underline{i}_2| \leq i_{\max} \tag{2.7}$$

with $\underline{i}_{1(2)}$ the positive (negative) sequence current phasor. In general, this limitation is too strict as the current limitation of the converter is valid in the *abc* frame, so a more advanced limitation could be applied in the *abc* frame. This limitation is based on [68]:

$$i_{\mathrm{a,max}} = \sqrt{i_1^2 + i_2^2 + 2 \cdot i_1 \cdot i_2 \cdot \cos(\alpha)} \tag{2.8a}$$

$$i_{\mathrm{b,max}} = \sqrt{i_1^2 + i_2^2 + 2 \cdot i_1 \cdot i_2 \cdot \cos\left(\alpha + \frac{4\pi}{3}\right)} \tag{2.8b}$$

$$i_{\mathrm{c,max}} = \sqrt{i_1^2 + i_2^2 + 2 \cdot i_1 \cdot i_2 \cdot \cos\left(\alpha - \frac{4\pi}{3}\right)} \tag{2.8c}$$

with $\alpha = \theta_{2i} - \theta_{1i}$ and $\theta_{1i(2i)}$ the angle of the positive (negative) sequence current phasor $\underline{i}_{1(2)}$[4].

It is seen that the maximum current depends on the value of α. For $\alpha = 0,\ \frac{2\pi}{3},\ \frac{4\pi}{3}$ the maximum current is equal to the one obtained by the straightforward limitation (2.7). For $\alpha = \frac{\pi}{3},\ \pi,\ \frac{5\pi}{3}$ however, the advanced current limitation (2.8) allows for a current that is 15.4% ($\frac{2}{\sqrt{3}}$) bigger than the current that is allowed with the straightforward limitation (2.7). As an illustration of the benefits of negative sequence injection and the possible gain of the advanced current limitation, a simple example is described below. In this example, a line-to-line fault with fixed fault voltages $\underline{u}_{1,\mathrm{fault}} = \underline{u}_{2,\mathrm{fault}} = 0.5\,\mathrm{p.u.}$ is considered. Only (positive and negative sequence) reactive current is injected into the fault, although in general active current could also be injected. This choice between active and reactive current and the priority between both depends on the grid requirements. A discussion on these alternatives is given in chapter 4 and 5.

In Figure 2.21, a line-to-line fault is applied at a system with only one CBDG unit. Both the positive and negative sequence schemes are given. The CBDG current limit is considered to be 1 p.u., although it can be designed for a slightly larger current. Using limitation (2.7), the currents will be as shown on the figure, resulting in a positive sequence voltage of 0.75 p.u. and a negative sequence voltage of 0.25 p.u. at the terminals of the CBDG unit. A conversion of these symmetrical component voltages to line-to-ground voltages with (A.1) leads to the following result: ($\underline{u}_a = 1\,e^{j\cdot 0^\circ}$ p.u., $\underline{u}_b = 0.66\,e^{j\cdot -139^\circ}$ p.u., $\underline{u}_c = 0.66\,e^{j\cdot 139^\circ}$ p.u.).

To briefly illustrate the benefits of the negative sequence current injection, Figure 2.22 shows the maximum current contribution when only positive sequence current is injected. The positive sequence voltage at the terminals of the CBDG unit is then boosted to 1 p.u., while the negative sequence voltage is the same as the negative sequence fault voltage, 0.5 p.u.. A conversion of these symmetrical component voltages to line-to-ground voltages gives the following result: ($\underline{u}_a = 1.5\,e^{j\cdot 0^\circ}$ p.u., $\underline{u}_b = 0.87\,e^{j\cdot -150^\circ}$ p.u., $\underline{u}_c = 0.87\,e^{j\cdot 150^\circ}$ p.u.). It is clear that an overvoltage results from this injection. In addition, the phase angles have a larger deviation when compared to the positive and negative sequence current injections in Figure 2.21. In this example, the assumption is made that the current injections do not influence the voltage at the fault location. In chapter 5, more realistic case studies will take this effect into

[4] An overview of the notations is also given in appendix A.

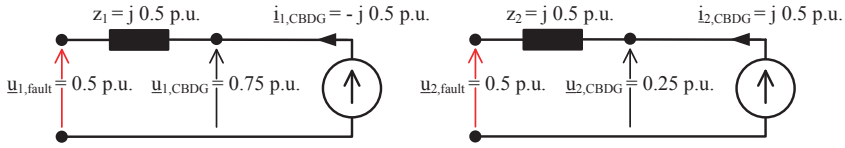


Figure 2.21: Line-to-line fault, maximum reactive current contribution of the CBDG unit with the straightforward current limitation (2.7)

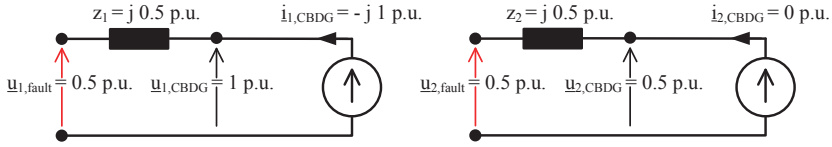


Figure 2.22: Line-to-line fault, maximum reactive current contribution of the CBDG unit with only positive sequence current injection

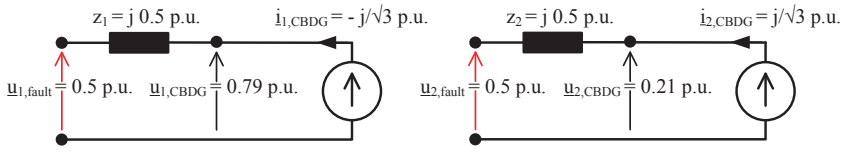


Figure 2.23: Line-to-line fault, maximum reactive current contribution of the CBDG unit with the advanced current limitation (2.8)

account. These case studies will confirm that blocking the negative sequence current and injecting positive sequence capacitive current leads to overvoltages.

The maximum current contribution according to the advanced current limitation (2.8) is shown in Figure 2.23. This illustrates that the advanced current limitation can obtain higher current injections, resulting in a higher positive sequence voltage (0.79 p.u.) and a lower negative sequence voltage (0.21 p.u.) at the terminals of the CBDG unit compared to the straightforward current limitation in Figure 2.21. A conversion of these symmetrical component voltages to line-to-ground voltages confirms that the voltage system is more balanced: ($\underline{u}_a = 1\,e^{j\cdot 0^\circ}$ p.u., $\underline{u}_b = 0.71\,e^{j\cdot -135^\circ}$ p.u., $\underline{u}_c = 0.71\,e^{j\cdot 135^\circ}$ p.u.). A similar conversion shows that the CBDG current limits are not violated: $|\underline{i}_a| = 0$ p.u., $|\underline{i}_b| = 1$ p.u., $|\underline{i}_c| = 1$ p.u..

Although the advanced current limitation (2.8) has some advantages, the

straightforward current limitation (2.7) is easier to implement in the control schemes. Therefore, the gain of the advanced current limitation is not always used, but it remains an interesting optimisation.

Influence of Negative Sequence Voltage Generation on the CBDG Voltage Limitation

From a given DC bus voltage, every converter can generate any AC voltage limited only by that DC bus voltage [52]. This relationship is determined by the modulation strategy that is used in the converter. Although this is not the focus of this dissertation, some considerations are given below as they will be used later in this work.

For a two-level VSC, Space Vector Modulation (SVM) is a common and efficient modulation technique [17, 52, 69]. It is able to generate higher voltages without overmodulation compared to the standard sinusoidal PWM. Without going into depth on these techniques, the basic idea is that any space vector within a certain circle with radius $u_{\max}$ can be generated without overmodulation [52,69]. As the combination of positive and negative sequence voltages results in a space vector that forms an ellipse with the longest axis equal to $|\underline{u}_1| + |\underline{u}_2|$ [39, 69] (see Figure A.3 in appendix A), this ellipse can only be within the circle when:

$$|\underline{u}_1| + |\underline{u}_2| \leq u_{\max}. \tag{2.9}$$

Other modulation techniques have other voltage limitations, but as SVM is a common modulation technique, this voltage limitation will be applied in chapter 5 to have realistic cases.

2.5 Conclusion

In this chapter, control systems for CBDG units during faults are described. The current controllers can control the positive and negative sequence current separately. A case study illustrates that by applying different setpoints, a different fault response is obtained. Thus, the fault behaviour of CBDG units is a design parameter. This knowledge will be used explicitly in chapter 4 and 5, where the benefits and drawbacks, for the grid, of different fault current contribution strategies are evaluated.

Although the suggested control systems can control the negative sequence current, there are some control aspects that require an optimisation and careful consideration in case negative sequence current injection is applied in actual

grids. In this chapter, the negative sequence phase angle detection and the voltage recovery after the fault are discussed. Other aspects, like the CBDG current limitation, could be optimised to achieve the maximum performance of CBDG units during faults.

Chapter 3

Simplified Calculation Techniques

> "All models are wrong, but some are useful."
>
> — George E.P. Box

3.1 Introduction

This chapter describes the simplified calculation techniques that are used in this dissertation. First, section 3.2 gives an overview of time based models that are described in literature, going from switched ElectroMagnetic Transient (EMT) models to Averaged Value Models (AVMs) and finally phasor models. Then, the linear network equation methods are described, starting with the traditional fault calculation method and its extensions for CBDG, going to the more advanced linear network equation methods, including the iterative methods. After this overview, section 3.3 illustrates the effectiveness of AVMs to model the detailed behaviour of CBDG units during faults. These AVMs are then used as a reference model to validate the Iterative Linear Network Equations Method (ILNEM). This method is described in section 3.4 and will be used for several fault studies in the following chapters. It is the simplest method capable of modelling the fundamental frequency fault behaviour of CBDG units. Therefore, section 3.5 concludes that the proposed method is

suitable to evaluate the trends of fault currents and fault voltages in grids with a high share of CBDG units.

3.2 Methods Described in Literature

Studying the impact of a large scale integration of DG in transmission and distribution grids, and developing mitigating measures, requires reliable simulation models for all types of DG. These models are readily available for IGs and SGs, but not for CBDG units. A special type of DG, the DFIG (used in type 3 WTs), is outside the scope of this dissertation, as explained in the introduction of this work. Therefore, these models are not discussed here, but some remarks are given in section 3.2.4.

In literature, both full time-domain switched and simplified models have been proposed to simulate the (fault) behaviour of CBDG. This section first gives an overview of time based methods and then of models based on linear network equations. All methods are discussed from the viewpoint of evaluating the fault current contribution strategies by CBDG units. This means the time range of interest ranges from about ten milliseconds (ms) to a few seconds after the fault[1].

3.2.1 Time Based Methods

Switched EMT Models

Traditionally, the most detailed power system simulations are the ElectroMagnetic Transient (EMT) simulations [71]. Here, the instantaneous values of the currents and voltages in the system are calculated, taking into account the non-linearities in the system. Specific to the simulation of power electronic components (VSCs) is that they use switching elements such as Insulated Gate Bipolar Transistors (IGBTs). This means that the model changes based on the state of these switches [16]. This results in a discontinuous model. Typical CBDG units have a switching frequency of several kHz [72], [73]. Therefore, a detailed switched model requires a time step that is considerably smaller to accurately calculate the variables during a switch cycle. In general, when there are several CBDG units, all switching actions in each CBDG unit change the simulation model. This obviously results in a very computationally intensive

[1]The maximal fault clearing time in the Belgian Federal Grid Code is 3.1 s or lower, depending on the voltage level [70]. When the transient stability of the system is part of the study, longer simulation times are required.

simulation. Both detailed models of IGBTs or ideal switches (on-off elements) can be used. There are several commercial software packages (e.g. PSCAD [63], PLECS [74]) that perform this type of simulation, but the simulations are in general very slow and only used for studies with a very limited amount of CBDG units. It is generally accepted that full time-domain switched models are computationally too intensive or time consuming for large system studies [72, 75–78]. These models are however required to study specific issues that are only visible when the switched models are used: e.g. harmonic interactions of the switching actions with the grid [71]. In the next section, a first simplification of the switched model is discussed.

Averaged Value EMT Models

Averaged Value Models (AVMs) are introduced to improve the simulation speed of EMT simulations with CBDG units. Compared to switched models, the AVM of a CBDG unit is continuous and (approximate) instantaneous values are calculated. The complete control system of the converter is simulated to capture the full behaviour of the CBDG unit, except the highest frequency variations related to the switching of the converter.

The IEEE Task Force on Dynamic Average Modelling has given a complete overview of AVMs in [72]. They explain AVMs as an approximation of the original system by averaging the effect of fast switching within a prototypical switching interval. The key idea is that the discontinuity of the switched models can be avoided and that the number of time steps can be reduced, resulting in much faster simulations.

In the AVM, one average value is defined over the length of a switching interval. For DC-AC converters (inverters), this cannot be applied directly according to [72], but a transformation to a synchronously rotating reference frame should be applied first. However, it is also possible to do the averaging in AC variables if the switching frequency is substantially higher than the output signal that is produced. This means that the signal that is modelled is considered as a DC signal (or low frequency signal) compared to the switching frequency. In [16], this approach is explained specifically for DC/AC half-bridge converters, two-level, three-phase VSCs and three-level, three-phase, Neutral-Point Clamped (NPC) VSCs. All AVMs have the advantage that they are continuous and capable of using much larger time steps than the switched, discontinuous models [71, 72].

In this dissertation, the AVMs according to [16] are considered. Instead of modelling the switching actions, controlled voltage sources apply voltages determined by the reference signal of the control system to the grid. This

technique assumes that the voltage that the control system wants to obtain is generated by the VSC. This was also mentioned in [79]: if the switching frequency is high enough and the output filter is designed correctly, the switching harmonics are attenuated. The lower frequency components of the reference voltage and the generated voltage of the converter are then equal. As the AVMs model the low frequency variations accurately, they also take into account the low frequency behaviour of the control system. The control system of the converter is simulated completely or in a simplified form to allow this.

Reference [76] mentions that an AVM does not depend on the converter topology or the modulation technique, but [80] is more careful in this regard, and states that, under simplifying assumptions, the model of the conventional two-level VSC can be deduced from that of the three-level NPC VSC.

There are however some drawbacks to AVMs. Compared to full time-domain switched models, information on high frequency components (e.g. harmonics) is lost [73]. Reference [73] states that the AVM is valid up to about one-third of the converter switching frequency, while [81] states that the AVM is valid up to half of the switching frequency. In [79] an important condition is added: an AVM is only valid if the frequencies in the reference signal are much smaller than the resonance frequency of the filter.

In section 3.3, an illustration of AVMs is given to illustrate that they are capable of modelling the control behaviour of CBDG units during faults. The significant gain in simulation speed is also discussed there. Afterwards, AVMs will be used in section 3.4 to validate the iterative method that is introduced there.

Phasor (RMS) Models

Simulations that calculate the time-varying phasor values of the variables instead of the instantaneous values are often referred to as Root Mean Square (RMS) or fundamental frequency simulations. In this case, the electromagnetic transients of the system are neglected and the focus is on the electromechanical events [82, 83]. Typically these models are used for transient stability studies and most of these simulations focus on balanced simulations, excluding the simulation of unbalanced faults. Commercial software such as DIgSILENT PowerFactory [84] also allows to simulate the phasor models in *abc* coordinates to allow for unbalanced simulations.

Dynamic phasor models [82, 85] were also introduced to simulate the control behaviour of CBDG units and asymmetrical faults by including higher frequency components [85] in the (dynamic) phasor models. The time step in the simulation can be increased compared to EMT simulations [82, 85]. These simulation

methods are very suitable for many simulations, but they still require an extensive model of the grid and the controllers of the generators and the CBDG units. A good overview of this technique is given in [82], including a discussion on the detailed modelling aspects (e.g. dynamic phasor models based on a fixed or a rotating reference frame).

This dissertation does not treat these RMS or dynamic phasor models further, but they are absolutely necessary for a large number of studies as they are more accurate than the linear network equation methods that are described below, but at the same time they can be much faster than EMT simulations [82, 83].

3.2.2 Linear Network Equation Methods

In the past, linear network equation methods were developed to calculate fault currents and fault voltages approximatively. These methods are much faster than the time-based methods and also need much less information about the network components. Nevertheless, they are able to provide a good accuracy. Many standards for fault calculations use this type of calculation method and these standards are commonly used in industry.

In this section, first the traditional fault calculation method is briefly discussed. From this discussion, it is clear that the standard methods are not capable of taking the fault behaviour of CBDG units into account. Afterwards, several improvements of these methods, to take the rising share of CBDG units into account, are discussed.

Traditional Fault Calculation Method

The traditional fault calculation method according to the (European) International Electrotechnical Commission (IEC) 60909 standard [86] is described in several textbooks [87–89]. This method solves linear equations to obtain a phasor solution of a linear network. Similar methods are described in [24]. The American National Standards Institute (ANSI)/IEEE C37.010 and C37.13 standards are also similar [89]. The fault conditions are applied to the network, where all voltage sources are determined by the prefault load flow or, alternatively, the load flow is not performed, but correction factors are applied to the voltage sources and the impedances to calculate the maximal or minimal fault currents. When accurate voltages during the faults are required, the method without the correction factors is more appropriate [86].

For unbalanced faults, the network is split into symmetrical components and the fault conditions are translated to conditions in symmetrical components. For

the most common faults, this leads to a simple connection of the symmetrical schemes [24, 87–89].

To solve these networks, often superposition is applied: the load flow before the fault is added to the situation during the fault. This assumes that all sources in the network are linear sources. It must be stressed that both the treatment in symmetrical components and the superposition principle are not required to calculate the fault currents. Especially when using a computer, the computational benefit is small or negligible for linear equations[2].

Models for conventional generation are readily available (IG, SG). On the contrary, there are no standardised models for CBDG units, whose fault behaviour is completely determined by the control system, as was explained in chapter 2. The IEC standard even disregards all static converters, except reversible static converter-fed drives [86].

Extensions to the Traditional Fault Calculation Method

The first logical extension to this method is to provide a CBDG unit model. Several models are suggested in literature. All these models have in common that an assumption on the fault behaviour of CBDG units is made.

The simplest technique, described in [92], considers the CBDG unit as a controlled current source and assumes the CBDG unit delivers its maximal fault current during faults. As the converter controls are assumed to produce only positive sequence currents, an equivalent sequence component representation is suggested, where both the negative and zero sequence impedances are infinite. Standard short-circuit calculation techniques [87] are then used and a positive sequence reactance is calculated iteratively, making sure the CBDG unit delivers its maximal fault current. If the calculation software is able to handle fixed current sources, the iteration process can be avoided. It is clear that this method is simple and that it allows calculating a safe estimate for the maximal fault current. However, in grids with a high share of CBDG units, a fault is never close to all CBDG units. Therefore, not all CBDG units inject their maximal current and this technique results in an overestimation of the total fault current. In addition, this technique does not provide an accurate evaluation of

[2]Roger Dugan, one of the authors of the OpenDSS software [90], explained this in the following way: "When computers only gave you 32-bit floating-point precision, the per-unit system naturally provided some normalisation that helped with precision of the power flow calculations. Today, with 64-bit, or greater, precision commonplace, this is no longer an argument for using the per-unit system. The per-unit system and symmetrical components were both invented in the pre-computer age to make hand calculations of 3-phase systems with transformers manageable. Computers, on the other hand, are perfectly happy doing the calculations in actual values and in actual 3-phase (or multi-phase) components." [91].

the network voltages, required for example for evaluating distance protection schemes.

Some sources [93, 94] propose a similar technique, but take into account that the maximal fault current is not the only parameter of importance and that, especially when considering protection settings, a more accurate method is required. Reference [93] proposes to use existing short-circuit analysis software, but to include a table lookup technique to relate the CBDG unit's injected current to the voltage at its terminals. The time dependency of the injected current can be taken into account in the tables, but this assumes that the voltage remains constant during the fault, which might not be a valid assumption in case of a high share of CBDG units. An alternative is given in [94], where a mathematical relationship determines the injected current: a positive sequence reactive current in function of the positive sequence voltage drop below 0.9 p.u. This paper only deals with a system with one CBDG unit. Both [93] and [94] assume a specific control strategy and provide improved accuracy, but unlike [94], the table method of [93] does not take into account the operating point of the CBDG unit prior to the fault. Implicitly, a control strategy that switches to a voltage based strategy during voltage dips is assumed. However, for some CBDG units like WTs, a transfer of active power may be required to facilitate FRT. This means that the injected current also depends on the operating point of the CBDG unit prior to the fault.

Other papers [75, 77] suggest alternative adaptations to the conventional short-circuit calculation methods. [75] determines iteratively which CBDG units go into current limit mode during a short-circuit, taking into account that most CBDG units are operated as PQ (= fixed active and reactive power) sources and only switch to a current limiting strategy to protect the power electronic components in the converter. This method does not simply assume that all CBDG units inject their maximal currents and is therefore able to calculate both voltages and currents during faults. Although different current limiting strategies are mentioned, only a predefined limit in the synchronously rotating reference frame is modelled, making this method only valid for this control strategy: e.g. it does not consider FRT active power transfer requirements during the fault. A positive sequence current source is proposed as the equivalent sequence component representation in the current limit mode to integrate the CBDG units in the calculation procedure. Reference [77] continues on this work. Here, an additional fault model for a current limiting strategy in the natural, fixed *abc* reference frame is developed. This model responds differently to asymmetrical faults: in three-leg converters negative sequence currents can also be injected and in four-leg converters both negative and zero sequence currents are possible. As the focus of [77] is on stand-alone grids, with low short-circuit powers, it assumes that all CBDG units in the network go into

current limiting mode, as the voltage drops during faults are large in weak grids. Both [75] and [77] could be combined, but it is clear that the control and certainly the current limiting strategy have a large influence on the fault model that has to be used. For each control/current limiting strategy a different fault model has to be developed to obtain accurate simulation results.

In all these methods some elements of the control system are taken into account, but as was explained in chapter 2, the control system determines the fault behaviour of the CBDG units. Therefore, the next methods will take the control system of the CBDG units into account. This will result in iterative methods.

Iterative Linear Network Equations Methods

An important assumption about many models is that they are completely linear. In chapter 2, it was demonstrated that the fault response of CBDG units can be controlled and is thus a design parameter. This means that the CBDG units cannot be considered as linear sources. Therefore, the Iterative Linear Network Equations Methods (ILNEMs) are developed. They also solve linear network equations, but at each iteration step the injected currents or the generated voltages of the CBDG units are changed in an outer loop that models (a simplified version of) the control system. This method still assumes that the SGs in the system are linear. It also assumes that the responses of the CBDG units are sufficiently fast and that the frequency in the system remains constant. Assessing changing rotor angles of SGs is for example not possible. For this, the RMS simulations described before should be applied. Nevertheless, this method is the simplest method that can take (the fundamental frequency behaviour of) the control system of CBDG units into account.

Methods that use these principles are described in literature [95, 96]. In this work, the method is fine-tuned and a calculation framework is developed and validated in section 3.4. More details on this method are provided there.

3.2.3 Choice of a Suitable Simulation Method

For most fault studies, the time range of interest ranges from about ten milliseconds (ms) to a few seconds. It is thus important that the simulation method accurately represents the behaviour of the CBDG units in this period. From chapter 2, it is clear that the control system determines the fault response of the CBDG units. As there are several control strategies for CBDG units, the simulation method has to take into account the most important aspects of the control system of the CBDG units. The AVMs preserve most dynamics in the

time range that is relevant for fault studies. They are considerably faster than switched models as is demonstrated in section 3.3 so they are very suitable to investigate the performance of control systems.

Although the AVMs are significantly faster than the switched models, they are slower than the ILNEM. In addition, an EMT simulation model with AVMs requires many details on the grid, the generators and the CBDG units. Therefore, it seems logical to investigate whether a simpler method, like the ILNEM can be used to see the trends of different control strategies. After validation, this method would also allow to simulate larger grids. The main advantage of AVMs is that the complete control system can be modelled in a straightforward way. For the ILNEM, outer loops have to model the behaviour of the control system. In addition, the ILNEMs assume that the CBDG unit injects mainly fundamental frequency currents (not excluding unbalanced fault currents). So first the performance of the control system should be verified with AVMs. Afterwards, other simulation methods like the ILNEM can be used to achieve faster simulations. The simpler linear network equation methods are not capable of modelling the control behaviour of CBDG units and are therefore not suitable for the studies of the following chapters. As a compromise between EMT simulations and the ILNEM, the RMS simulations are a good alternative. These simulations also require a model of the control system, but focus on the phasor values. This type of models is also required when the transient stability of the generators in the system has to be checked, but an EMT simulation is computationally too intensive. In the ILNEM, it is implicitly assumed that the transient stability of the system is already checked through other simulations. In this dissertation, the ILNEM is used after a verification with AVMs.

3.2.4 Remark on Simulations with DFIGs

In chapter 2, it is demonstrated that the fault behaviour of CBDG units is a design parameter. DFIGs however, have a fault behaviour that is also determined by the direct coupling part of the DFIG with the grid. Therefore, the ILNEM cannot be (directly) applied for DFIGs. In some cases, when the fault behaviour of the DFIGs can be controlled, the ILNEM can be used for DFIGs. This is clarified further in chapter 4, section 4.2.5, for balanced faults. For unbalanced faults, the ILNEM cannot be used for DFIGs. This is explained in chapter 5, section 5.2.4. Some papers [97–99] also deal with simplified, approximate estimations of the (maximal) short-circuit currents of DFIGs. These are however not integrated in a calculation framework. In literature, often RMS or dynamic phasor simulations are used for DFIGs to avoid the time-consuming EMT simulations [100–103]. E.g. a reduced-order phasor based simulation model is suggested in [104].

3.3 AVM as Reference Model

This section describes some examples from literature (section 3.3.1) and the simulations performed in publication [48], presented at the IEEE PEDG conference in 2012 (section 3.3.2). In [48], switched models and AVMs are compared to illustrate that AVMs model the behaviour of the control system accurately. The control system that is simulated is less advanced than the DDSRF controller described in chapter 2. However, this illustrates that the shortcomings of a control system can be shown with an AVM. In section 3.4, these AVMs are used as a reference model for the ILNEM. These simulations also demonstrate that AVMs offer an increased efficiency of the simulations compared to switched models. This increased efficiency is required to simulate grids with multiple CBDG units, as each CBDG unit that would be added with a switched model would unnecessarily increase the complexity of the simulation, resulting in infeasible simulation times for larger systems.

3.3.1 Examples Described in Literature

There are several examples of AVM applications in literature. Three examples are mentioned here briefly.
Reference [76] describes AVMs for HVDC transmission systems with VSCs. The AVMs are reported to give an accurate replication of the dynamic behaviour of the IGBT based switched models. Simulation examples in [76] show that AVMs give a significant gain in simulation time: gains of more than 20 times are easily reached. Another example of AVMs is found in [105]: here an AVM is applied to increase the simulation speed of a DFIG. An AVM is used for the VSC feeding the rotor circuit of the DFIG. The simulation gains that are reached depend strongly on the induction machine model, but it is clear that the AVM enables a serious reduction in simulation time. The last example of an AVM application is found in [73]: here the AVMs are mentioned as an alternative to switched models for faster simulations in power system studies of three-phase PV systems.

3.3.2 Example of an AVM

Simulation Model

To compare the fault response of a switched model and its AVM, a simulation model is built in Matlab/Simulink [106,107] with the PLECS blockset [74]. The electrical part of the model (grid and CBDG unit) is modelled in PLECS and

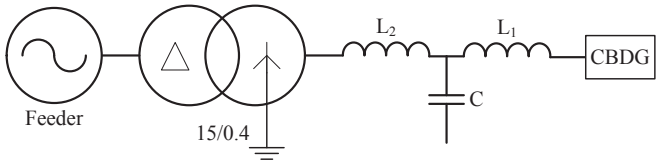


Figure 3.1: Grid model

Table 3.1: Grid data

Element	**Property**	**Value**
System feeder	U_{nom}	15 kV
	S_{sc}	200 MVA
	X/R ratio	10
	f_{nom}	50 Hz
Transformer	S_{nom}	2.5 MVA
	U_{nom}	15 kV / 400 V
	Vector group	Dy11 (solidly earthed)
	u_k	6%
CBDG unit	S_{nom}	60 kVA
	$U_{nom,DC}$	800 V (constant)
	$f_{carrier}$	10 kHz
Filter	L_1	2.3 mH
	L_2	0.9 mH
	C	8.8 µF (Y connected)

the converter control system in Simulink. The PLECS configurable subsystems allow to create one model, with one Simulink control system, and to select the appropriate configuration for the converter: switched or AVM. The grid model is shown in Figure 3.1. It consists of a system feeder, modelled as a voltage source and an impedance, a delta-wye transformer and a LV VSC unit with an LCL filter. The grid data is shown in Table 3.1. The switched model is the standard three-phase, two-level IGBT converter model of PLECS. Both the IGBTs and the reverse diodes are ideal in this model. PLECS needs only six internal switches to represent this converter, so the simulation of this model is already faster than the simulation of a model that specifies all electrical parameters and non-linearities of the IGBTs and diodes. The AVM is shown in

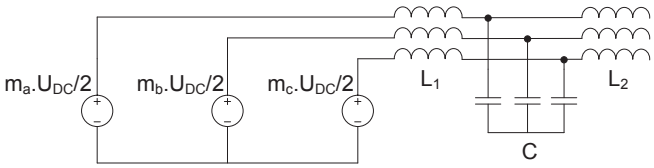


Figure 3.2: AVM and filter of the simulation model

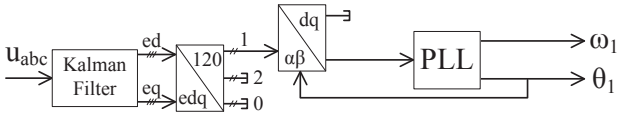


Figure 3.3: Advanced PLL for grid synchronisation

Figure 3.2 and consists of voltage sources $m_i \cdot \frac{U_{\mathrm{DC}}}{2}$ in each phase ($i = a, b, c$), where the modulation indices m_i are controlled by the converter control system in Simulink. This model is based on the averaged ideal three-phase VSC model that is discussed in section 3.2.1 and explained in detail in [16]. The DC bus voltage of the CBDG unit is modelled as a constant DC voltage source. Additional elements can be added to include switching and conduction losses [16]. The DC power balance can be included as well. As can be seen in Figure 3.2, the AVM only replaces the switched model, the filter is not included in the AVM.

Control Strategy

The CBDG unit has a SRF current control system, as discussed in chapter 2 (section 2.2.2, Figure 2.4). The current references are kept fixed, and are therefore independent of the voltages in the system. In the results shown next, i_{ref} is the current reference, i_{meas} is the current measured at the output of the CBDG unit (before the filter), u_{grid} is the voltage measured at the grid side of the CBDG unit (after the filter) and u_{ref} is used to determine the modulation indices m_i of the converter (switched model or its AVM). The grid voltage phase angle, required to transform the three-phase variables abc to the voltage oriented reference frame variables dq, is estimated with a PLL.

Two PLL configurations are considered. In the first configuration, shown in Figure 2.5, a simple PLL without positive and negative sequence separation is implemented. The second, more advanced, PLL configuration uses positive and

negative sequence separation. A slightly different implementation compared to the implementation of Figure 2.6 is used. The PLL scheme is illustrated in Figure 3.3. In a first step, the fundamental frequency components of the *abc* line-to-neutral voltages are determined with a Kalman estimator, as was set forth in [108] for single phase applications. These voltages are then transformed into positive, negative and zero sequence components with the help of transformations similar to [109]:

$$\begin{bmatrix} ed_1 \\ eq_1 \\ ed_2 \\ eq_2 \\ ed_0 \\ eq_0 \end{bmatrix} = \frac{1}{3}\frac{\sqrt{3}}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ 0 & 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 1 & 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ 0 & 1 & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} ed_a \\ eq_a \\ ed_b \\ eq_b \\ ed_c \\ eq_c \end{bmatrix} \tag{3.1}$$

where $ed_{a,b,c}$ are the fundamental frequency components and $eq_{a,b,c}$ are their quadrature components as determined by the Kalman estimator. This is an application of the instantaneous symmetrical components expressed with a 90° phase shift, as described in [57]. Because the q components lag the d components in this implementation, the signs in the equation mentioned here are different. The factor $\frac{\sqrt{3}}{\sqrt{2}}$ arrives from the equivalence with the control system variables $\alpha\beta$ in this specific implementation. The positive sequence components ed_1 and eq_1 are then used instead of the $\alpha\beta$ signals to determine the phase angle reference in the PLL. The negative sequence angle is not estimated in this implementation as only positive sequence currents will be injected in this example. This latter PLL configuration is referred to as the advanced PLL, the other PLL configuration is referred to as the basic PLL in the discussion of the results. The current control loop is the same in both configurations.

Simulation Results

Several fault types have been simulated. For all fault types, the AVM fault response is a good approximation of the switched model fault response. Here, only the results of a three-phase and a line-to-line fault (between phase b and c) are shown. The fault always occurs at the LV side of the transformer at $t = 0.5\ s$.

Figure 3.4 shows the fault response of the CBDG unit to a three-phase fault. The basic PLL configuration is used, but as a three-phase fault results in a balanced situation, this does not result in problems. The voltages at the LV and MV side of the transformer are shown in Figure 3.4a-3.4b. The other figures

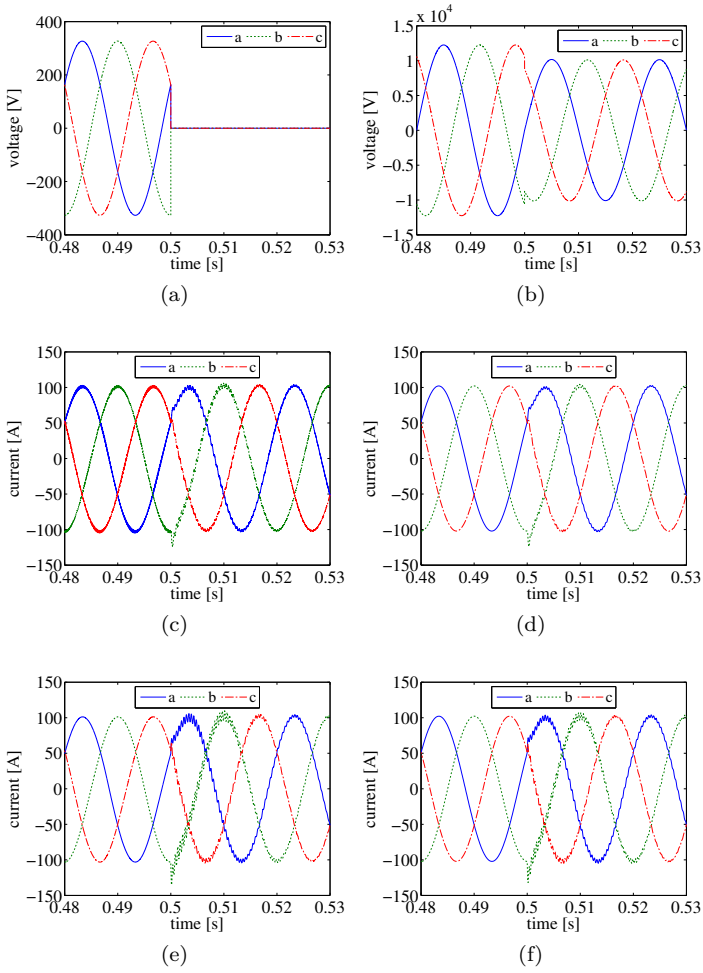


Figure 3.4: Comparison between the switched model and its AVM for a three-phase fault, with the basic PLL configuration: (a) Voltage at the LV side and (b) at the MV side of the transformer. (c) Converter output current (before the filter) of the switched model and (d) its AVM. (e) Converter output current (after the filter) of the switched model and (f) its AVM.

compare the switched model (on the left) with its AVM (on the right). The current responses of both models are very similar. As was mentioned previously, the current reference is kept fixed in the control system. This explains why the current does not increase during the fault. As this is a simulation, the PLL is able to track the phase angle, even for very small voltages during the fault. In reality, the accuracy of the PLL is of course limited by measurement errors.

Next, a line-to-line fault is applied to the same system. The results are shown in Figure 3.5, which shows the same order of plots as Figure 3.4. Again the current responses of both models are very similar. Figure 3.6 shows zoomed parts of Figure 3.5. The switched model and its AVM are plotted on top of each other to show their close resemblance. Figure 3.6a and 3.6b show the current in phase a before and after the filter. Since the current after the filter is the most relevant for fault studies, the phases b and c are shown in Figure 3.6c-3.6d. It is clear from these figures that the basic PLL is not able to accurately track the phase angles of the voltages. This is because the negative sequence voltages appear as second order harmonics after the transformation from abc to dq coordinates [17, 110]. The basic PLL is not able to deal with these second order harmonics and the phase angle reference becomes distorted. The AVM accurately reproduces this as it is an effect related to the voltages in the grid during the fault. This problem and solutions to track the phase angles of the voltages during unbalanced faults were discussed in chapter 2. The main idea is to track the positive sequence and negative sequence separately. This is done in the advanced PLL as explained before. Subsequently, this PLL configuration is included in the simulation models and the same line-to-line fault is applied to the system at the same time. Again, the switched model is shown next to its AVM in Figure 3.7. Because the CBDG unit is small (2.4% of the transformer rating), it does not noticeably influence the voltages in the system, as can be seen by comparing the voltages during the fault in Figure 3.5 and 3.7. But as expected, the converter control system responds differently to the fault: the currents are not deformed and they are hardly influenced by the fault because the current reference is unaltered. Again the AVM fault response closely resembles the switched model fault response. This illustrates that the AVM simulates the control system and allows to investigate the influence of the converter control systems in grids with a high share of CBDG units.

Accuracy of the AVMs

The AVM techniques that are applied are generic, see section 3.2.1, so they are also valid for larger CBDG units with VSCs, connected to the MV grid. These units often have lower switching frequencies. From the discussion in section 3.2.1, it is clear that the AVM will differ more from the switched model

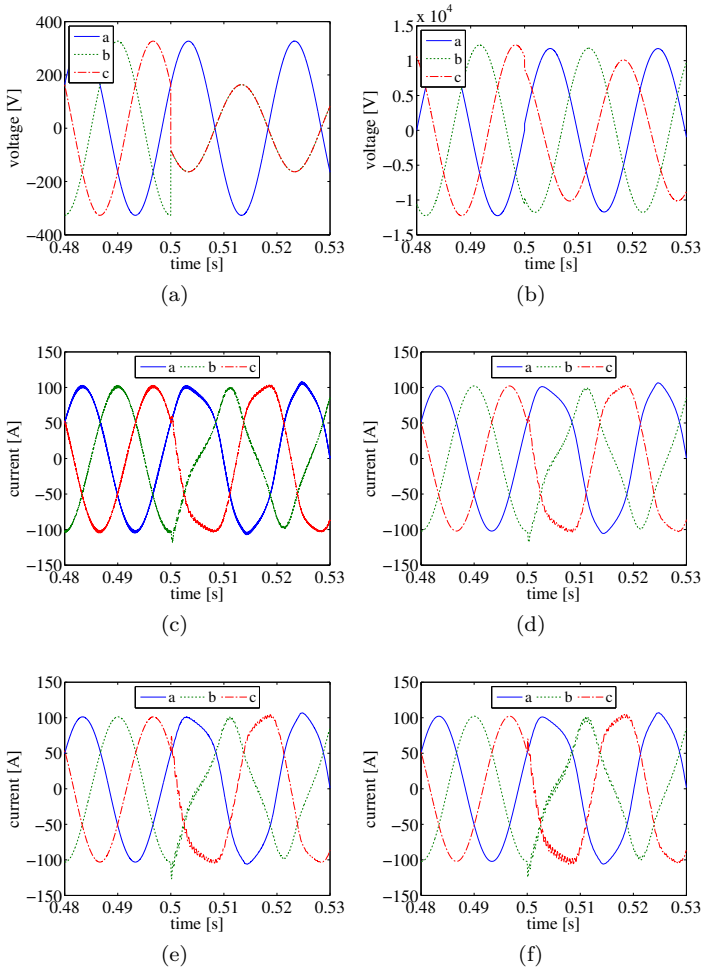


Figure 3.5: Comparison between the switched model and its AVM for a line-to-line fault (phase b and c), with the basic PLL configuration: (a) Voltage at the LV side and (b) at the MV side of the transformer. (c) Converter output current (before the filter) of the switched model and (d) its AVM. (e) Converter output current (after the filter) of the switched model and (f) its AVM.

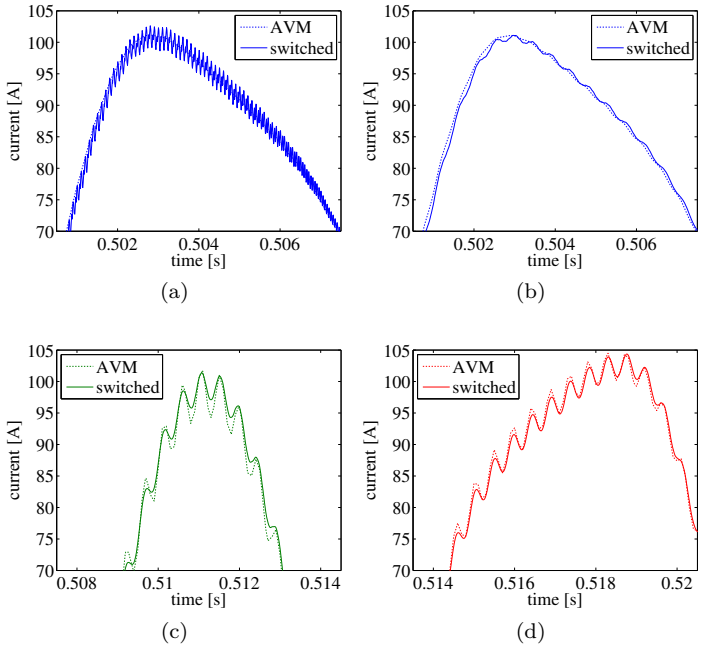


Figure 3.6: Detailed comparison between the switched model and its AVM for a line-to-line fault (phase b and c), with the basic PLL configuration: (a) Converter output current (before the filter) of phase a. (b), (c) and (d) Converter output current (after the filter) of the three phases.

in this case. But in general, the switching frequencies are higher than 1000 Hz (20 times the fundamental frequency in 50 Hz grids) and AVMs give a good approximation. As an illustration, the simulation of a line-to-line fault with the basic PLL configuration is repeated with a switched model of 5000 Hz. The filter is the same as in the previous model, although in principle a different switching frequency requires a redesign of the LCL-filter. The output current of the switched model of the CBDG unit is plotted in Figure 3.8 next to its AVM, which is of course the same as the AVM of Figure 3.5.

All examples illustrate that AVMs give a very good approximation of the fault response of the switched models. Only when the higher harmonics are important, e.g. when the switching frequency harmonics interact with other parts of the system (e.g. resonance), the AVMs are not sufficiently accurate. For a properly designed CBDG unit, this is not the case and the AVM technique is then a suitable technique for approximating the switched model.

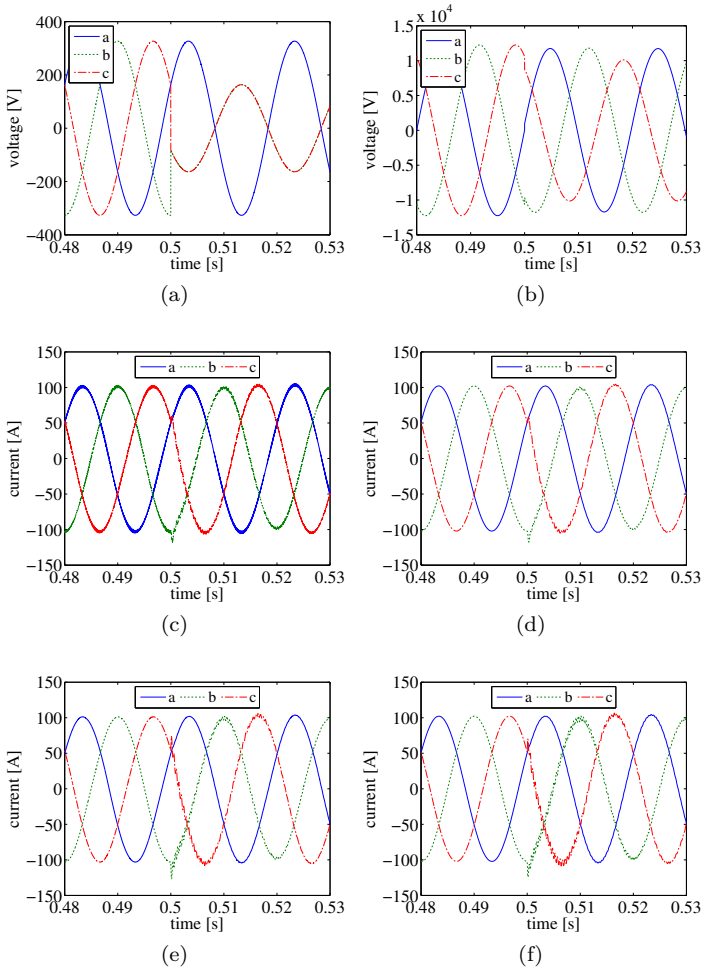


Figure 3.7: Comparison between the switched model and its AVM for a line-to-line fault (phase b and c), with the advanced PLL configuration: (a) Voltage at the LV side and (b) at the MV side of the transformer. (c) Converter output current (before the filter) of the switched model and (d) its AVM. (e) Converter output current (after the filter) of the switched model and (f) its AVM.

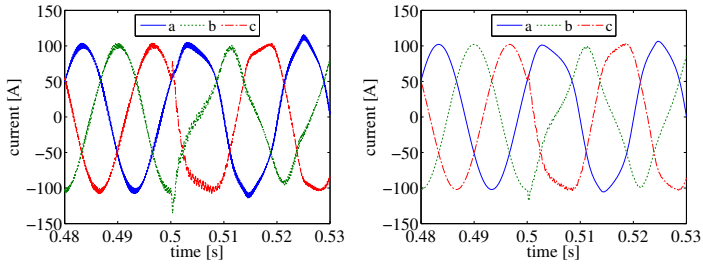


Figure 3.8: Comparison between the switched model and its AVM for a line-to-line fault (phase b and c), with the basic PLL configuration: (a) Converter output current (before the filter) of the switched model at 5000 Hz and (b) of its AVM.

Simulation Speed

For the basic PLL configuration, simulating the AVM for 3 s required around 11.8 s, while the switched model required around 194 s. The simulation duration of 3 s was chosen because it is around the maximal time that is required in protection studies (see section 3.2). For the advanced PLL configuration, the AVM simulation takes about 13.1 s, compared to about 225 s for the switched model. The AVM is thus significantly faster (factor 16-17) than the switched model, although the same computer was used, and both models used the same Simulink control system. These gains in simulation speed are similar to the gains reported in [76]: the gains are a bit smaller, but in [76] the comparison is made with a switched model that contains non-ideal diodes and a snubber circuit. Here, the PLECS switched model only contains ideal diodes.

3.4 Iterative Linear Network Equations Method

This section describes the Iterative Linear Network Equations Method (ILNEM). First, the method and its background are described. Afterwards, the framework that is used in this dissertation is introduced. Next, the method is validated by comparing it with AVM simulations. Finally, some limitations of the proposed method are summarised.

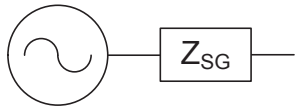


Figure 3.9: SG model in the positive sequence scheme

3.4.1 Method Description

The grid representation is very similar to the traditional fault calculation methods used in the IEC and ANSI/IEEE standards. Lines and transformers are represented by impedances. The loads are also represented by impedances to obtain a fully linear system, but alternative load models can be integrated in the method. The source models of the SG and the CBDG unit are discussed below.

SG Model

The classical model [32, 111] of a SG is constructed in symmetrical components. In the positive sequence, it is a voltage source and an impedance, Figure 3.9. Usually, the impedance Z_{SG} is mainly reactive ($j \cdot X_1$) and often, the resistive part is neglected. To take into account the time variance of the SG, the reactance can be changed from the subtransient reactance $X^{''}$, over the transient reactance $X^{'}$, to the steady state reactance X. The corresponding voltage source is always altered to obtain the same initial load flow ($E^{''}$, $E^{'}$ or E). This model does not take any action of the Automatic Voltage Regulator (AVR) into account [32]. There is also no saliency in this model ($X_d = X_q = X$, $X_d^{'} = X_q^{'} = X^{'}$ and $X_d^{''} = X_q^{''} = X^{''}$ is assumed), although a synchronous machine always has transient saliency [32]. The motion equations of the SG are not modelled. Therefore, this model assumes only minor changes to the relative angles of the machines in the system. This model will be more accurate for shorter fault durations and higher inertia constants of the SGs. In the negative sequence scheme, the model of the SG is a reactance with the value X_2, defined by:

$$X_2 = \sqrt{X_d^{''} \cdot X_q^{''}} \tag{3.2a}$$

$$\approx \frac{X_d^{''} + X_q^{''}}{2} \tag{3.2b}$$

where the (3.2b) is the Taylor approximation, assuming $X_d^{''} \approx X_q^{''}$. This negative sequence reactance is considered time independent. The zero sequence

impedance of the SG is machine dependent and also depends on the connection of the machine. In most cases, the step-up transformer of the SG blocks the zero sequence scheme and in those cases, the zero sequence impedance of the SG does not play a role in the calculations.

When looking at three-phase faults, a theoretic expression for the fault current of a SG in phase a is derived in [32]:

$$\begin{aligned} i_a = &- \left[\left(\frac{E_{q0}^{''}}{X_d^{''}} - \frac{E_{q0}^{'}}{X_d^{'}} \right) \cdot e^{-\frac{t}{T_d^{''}}} + \left(\frac{E_{q0}^{'}}{X_d^{'}} - \frac{E_{q0}}{X_d} \right) \cdot e^{-\frac{t}{T_d^{'}}} + \frac{E_{q0}}{X_d} \right] \dots \\ &\cdot \sqrt{2} \cos(\omega t + \gamma_0) + \dots \\ &\left[\left(\frac{E_{d0}^{''}}{X_q^{''}} - \frac{E_{d0}^{'}}{X_q^{'}} \right) \cdot e^{-\frac{t}{T_q^{''}}} + \frac{E_{d0}^{'}}{X_q^{'}} \cdot e^{-\frac{t}{T_q^{'}}} \right] \cdot \sqrt{2} \sin(\omega t + \gamma_0) + \dots \\ &\sqrt{2} \cdot \frac{U_{g0}}{2} \cdot e^{-\frac{t}{T_a}} \left[\left(\frac{1}{X_d^{''}} + \frac{1}{X_q^{''}} \right) \cdot \cos(\gamma_0 + \delta_g) + \dots \right. \\ &\left. \left(\frac{1}{X_d^{''}} - \frac{1}{X_q^{''}} \right) \cdot \cos(2\omega t + \gamma_0 + \delta_g) \right] \end{aligned} \tag{3.3}$$

where subscript 0 indicates prefault quantities, U_g is the terminal voltage and δ_g is the angle between the q axis and U_g. The DC and the double frequency term are not modelled in the phasor model by definition. The double frequency component is small when the subtransient saliency is limited, which is the case for most generators [32]. Because the classical model neglects saliency, and as in general $X_q^{'} > X_d^{'}$ and $T_q^{'} < T_d^{'}$, it gives an overestimation of the fundamental frequency fault current. For smaller times and limited subtransient saliency, the error of the classical model is limited. In general, the assumptions of this model are acceptable, but when a better accuracy is required, it is recommended to switch to time based phasor (RMS) simulations [111]. Derivations for a line-to-line fault are also given in [32] and lead to similar conclusions: when the saliency is limited, the classical model gives an acceptable approximation.

CBDG Model

The CBDG units are modelled either as a current source or as a voltage source with an impedance, Figure 3.10. This model is used in both the positive and in the negative sequence. In both cases, the CBDG unit is current controlled by an outer loop representing the control system. In case of a current source, the injected current is changed by the control system and in case of a voltage

Figure 3.10: CBDG model

source, the current is controlled by adjusting the value of the impedance and/or the voltage source. Chapter 2 showed that the fault behaviour of a CBDG unit is determined by the control system. Therefore, when the control behaviour is modelled correctly, this model accurately represents the CBDG unit.

3.4.2 Calculation Framework

Here, the framework and some implementation aspects of the ILNEM method are clarified.

Up till now, the form of the equations is not specified, except that they should be linear. In general, the grid can be represented in its three-phase form or in symmetrical components. Symmetrical components have the advantage that the matrices can be decoupled or approximately decoupled when the full grid matrix is cyclic symmetrical [88]. If this full grid matrix is not cyclic symmetrical, the positive, negative and zero sequence impedance matrix of the grid are coupled. In these cases, there is no real computational benefit. In addition, as explained in section 3.2.2, a modern computer has no issues in solving large sets of linear equations. Therefore, the grid is not modelled in symmetrical components, but in phase coordinates. The input data for the elements (SGs, lines, transformers, CBDG units, ...) can be provided in symmetrical components, but it is converted to phase coordinates in the model. An alternative implementation in symmetrical components is of course also possible.

This framework builds on the flexible object oriented Matlab framework code of the department [112]. This framework allows to create objects by defining their equations (relationships between variables potential and current) and their terminals (connection points). Methods for connecting and disconnecting objects are available. In addition, subcircuits allow to create more advanced grid elements by combining several elements or even subcircuits (e.g. a three-phase transformer is a subcircuit constructed with single phase transformers). This framework was used during this dissertation to model all standard grid components. This approach results in relatively sparse matrices. These matrices

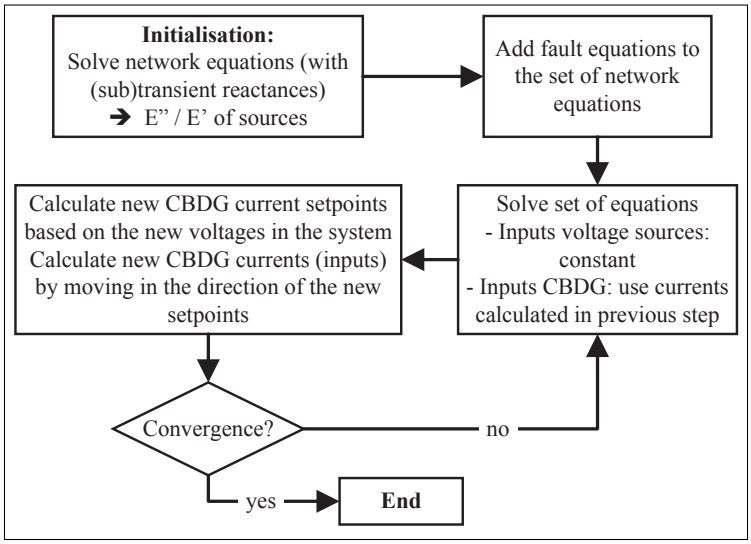


Figure 3.11: Flowchart of the calculation procedure

could be reduced, but this is not required as Matlab has efficient sparse matrix solvers.

Calculating short-circuit currents is straightforward by starting from a power flow result and then applying the fault condition. This makes the code very flexible as adding a connection or removing a connection allows creating several fault types. It is even possible to calculate simultaneous faults or faults between different voltage levels. The resulting code is checked by comparing power flow and short-circuit calculations without CBDG units with the results obtained by a commercial power system software (DIgSILENT PowerFactory [84]). The next section describes the validation of the code including CBDG units.

When there are CBDG units in the system, the grid has to be solved iteratively to include the control system actions of the CBDG units. The procedure is represented in the flowchart in Figure 3.11. The outer control loops determine the new currents (or voltage source - impedance combination) of the CBDG units. Although others [95, 96] have suggested similar methods, they have been demonstrated only with a limited number of CBDG units. Applying a straightforward iteration, where the new setpoint is applied immediately, does not work when there are several CBDG units in the network. Every CBDG unit influences the voltage and the new voltages cause new setpoints for the CBDG units. This keeps on repeating and no convergence occurs. In this work, the method is fine-tuned by moving gradually in the direction of the new

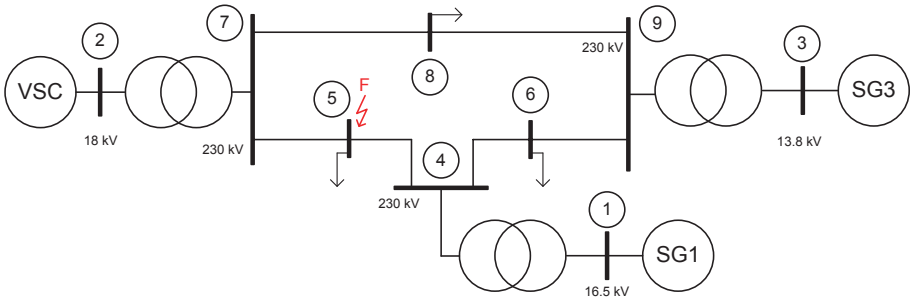


Figure 3.12: Simplified system for model verification

Table 3.2: Load and generation data for the test system
(all values are given in the load sign convention)

	bus 1	bus 2	bus 3	bus 5	bus 6	bus 8
P [MW]	-124.1	-99.1	-94.5	125.7	90.5	100.6
Q [MVAr]	-65.1	-49.3	-28.3	50.3	30.2	35.2

setpoints (e.g. steps of 1-2 % of the current rating of the CBDG unit). This comes at a cost of more iterations (around 100 iterations are then required), but guarantees convergence to a realistic solution. The use of more advanced, dynamic step sizes could reduce the required number of iterations, but this is not implemented in this dissertation.

3.4.3 Validation

In this section a validation of the ILNEM is made. First the test system is introduced. Afterwards, balanced and unbalanced faults are applied to the system. The ILNEM method is compared with an EMT simulation in PSCAD [63]. The CBDG unit is represented by an AVM in the EMT simulations. The validation with a balanced fault is also reported in publication [49], presented at the IEEE Powertech conference in 2015.

Test System

A nine bus system, inspired on the Western Electricity Coordinating Council (WECC) nine bus system with three synchronous generators (SG1-SG3) [113], but with modified line lengths, is used as test system. SG2 is replaced by a VSC

unit with the same nominal power as SG2. The generator, transformer and line data are given in appendix B, Tables B.1, B.2 and B.3. The load and generation data is given in Table 3.2 (load sign convention). In the load sign convention, a load (positive P) is inductive when Q is positive and the generation (negative P) is capacitive when Q is negative.

In the EMT model, the speed of the SGs is kept fixed to exclude the influence of the mechanical equations and the inertia of the sources during the validation. The saliency of the SGs is modelled and is one of the main reasons for divergence of the results of the SGs for longer fault durations. The VSC unit responds to the voltage dip at its terminals by injecting reactive currents: only positive sequence reactive currents during balanced voltage dips and both positive and negative sequence reactive currents during unbalanced voltage dips. The exact voltage support strategy of the VSC unit is not important for this validation. For now, it is important that both the EMT simulation and the ILNEM calculation correspond with each other. The voltage support strategies are discussed further in chapter 4 and 5.

Balanced Faults

A three-phase fault is applied to bus 5. First, an ideal fault (without fault impedance) is applied. The results of both the EMT simulation and the ILNEM calculation are compared by plotting them in the same graph, see Figure 3.13, 3.14 and 3.15, for SG1, VSC and SG3. In order to compare the instantaneous values and the phasor values, all instantaneous values are scaled with a factor $\sqrt{2}$. To take the time dependence of the solution into account, the ILNEM calculation is made three times: with the subtransient (solid horizontal line), the transient (dotted horizontal line) and the 200 ms reactance values (dash-dotted horizontal line) for the SGs. This 200 ms reactance value is calculated based on the transient reactance, the steady state reactance and the short-circuit transient time constant [32].

Of course, the DC behaviour is not modelled in the ILNEM. When excluding this, it can be seen that the ILNEM calculation gives a good approximation of both currents and voltages during a balanced fault. SG3 is a salient pole generator and has a larger transient saliency compared to SG1. Therefore, the model used for a SG will start to deviate more quickly for SG3 than for SG1.

Afterwards, a three-phase fault with an impedance $21.9 + j \cdot 52.9\,\Omega$ is applied. This represents a fault with an impedance of $5\,\Omega$ behind a transformer (200 MVA, 230/110 kV, $u_k = 20\%$). The results of both the EMT simulation and the ILNEM calculation are compared in Figure 3.16, 3.17 and 3.18 for all sources. The DC component is smaller, simplifying the interpretation of the graphs. Also for

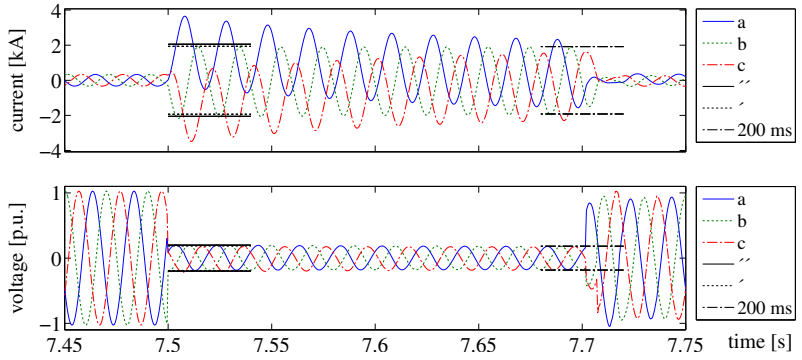


Figure 3.13: (Scaled) SG1 current and line-to-ground voltages at bus 4 during a three-phase fault without fault impedance at bus 5 (ILNEM ↔ EMT)

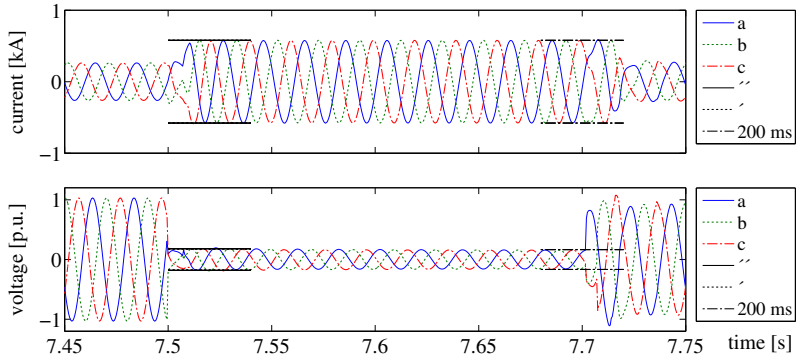


Figure 3.14: (Scaled) VSC current and line-to-ground voltages at bus 7 during a three-phase fault without fault impedance at bus 5 (ILNEM ↔ EMT)

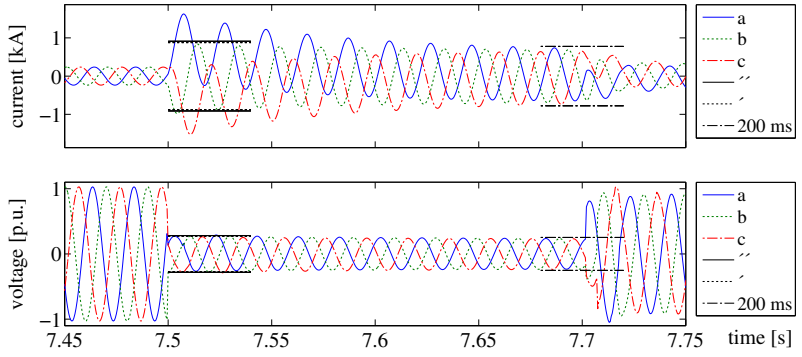


Figure 3.15: (Scaled) SG3 current and line-to-ground voltages at bus 9 during a three-phase fault without fault impedance at bus 5 (ILNEM ↔ EMT)

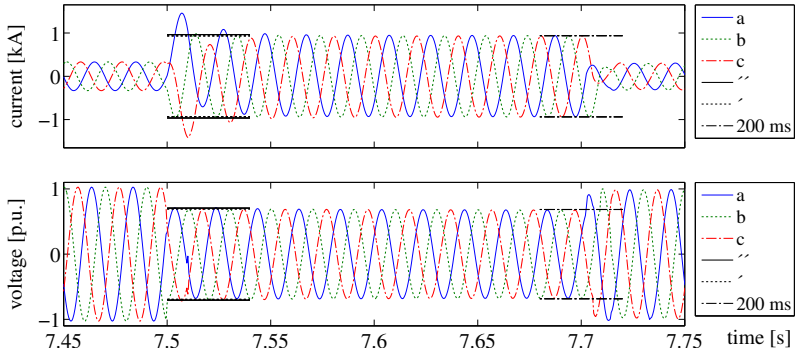


Figure 3.16: (Scaled) SG1 current and line-to-ground voltages at bus 4 during a three-phase fault with fault impedance at bus 5 (ILNEM ↔ EMT)

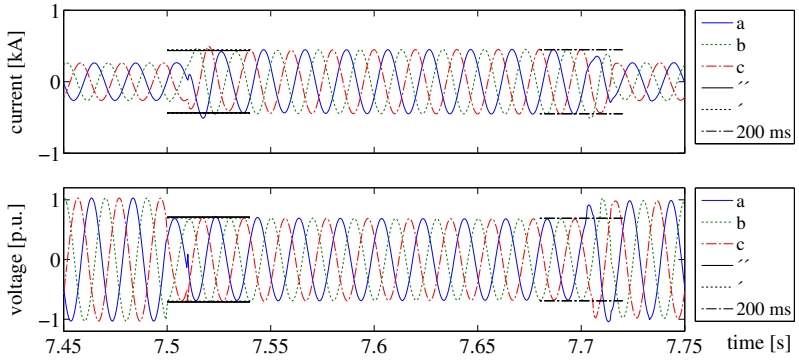


Figure 3.17: (Scaled) VSC current and line-to-ground voltages at bus 7 during a three-phase fault with fault impedance at bus 5 (ILNEM ↔ EMT)

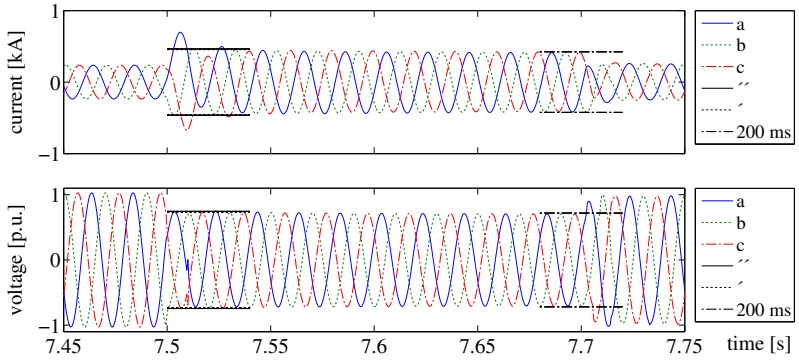


Figure 3.18: (Scaled) SG3 current and line-to-ground voltages at bus 9 during a three-phase fault with fault impedance at bus 5 (ILNEM ↔ EMT)

larger fault times, the accuracy of the model is higher. This is due to the fact that the total fault impedance, between the voltage source and the fault, has a relatively smaller part that varies over time. Only the generator impedance varies over time, the other elements, such as the lines and the fault impedance, remain constant. Therefore, the influence of a reduced accuracy on the generator impedances is smaller than for a fault closer to the generators.

Unbalanced Faults

Then line-to-line faults are applied to the test system. Now also the modelling of the negative sequence current injection by the VSC unit is evaluated. First, an ideal line-to-line fault at bus 5 is simulated in Figure 3.19, 3.20 and 3.21. As the results for each phase are different, the results from the ILNEM are represented in the corresponding color of the phase. Again the subtransient (solid horizontal lines), transient (dotted horizontal lines) and 200 ms value (dash-dotted horizontal lines) are represented[3]. When excluding the DC components, it is clear that there is a good correspondence between the EMT simulation and the ILNEM calculations. As a side remark, it is also clear from the EMT simulations that the voltage recovery after the fault and the angle reference switching at the start of the fault for the VSC unit are not fully optimised. This is discussed in chapter 2, section 2.4. These issues do not influence the validation of the ILNEM calculation as the system quickly stabilises after the changes of the reference angle and the ILNEM calculation is not used for evaluating the voltage recovery. Again, the transient saliency of SG3 causes a smaller accuracy for SG3 compared to SG1. The model is still reasonably accurate and therefore the voltages in the system are reasonably accurate. The corresponding voltage support of the VSC unit is therefore also accurate and the ILNEM calculation is a good approximation of the EMT simulation.

Afterwards, an ideal line-to-line fault is applied behind a transformer (200 MVA, 230/110 kV, $u_k = 20\%$) that is connected to bus 5. The results are given in Figure 3.22, 3.23 and 3.24. Again, similar conclusions can be drawn from the figure. The settling time for the VSC current is a bit slower compared to the previous simulations. However, the ILNEM calculation accurately predicts the settled values of the EMT simulation.

[3]The legends in these figures show black lines to indicate the line style of the different ILNEM results.

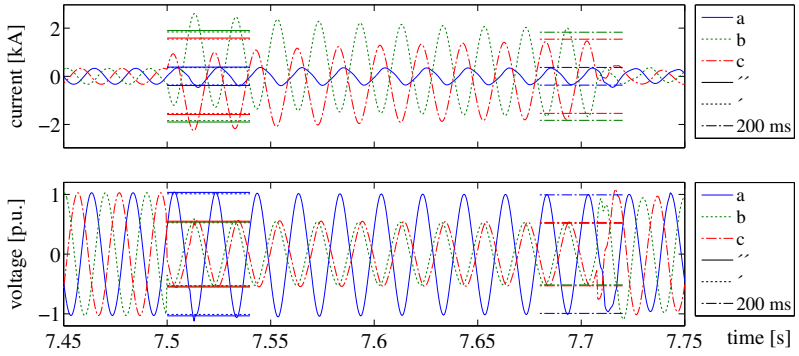


Figure 3.19: (Scaled) SG1 current and line-to-ground voltages at bus 4 during a line-to-line fault without fault impedance at bus 5 (ILNEM ↔ EMT)

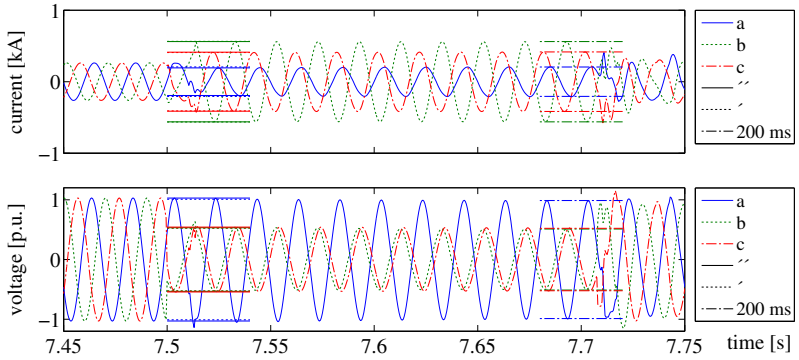


Figure 3.20: (Scaled) VSC current and line-to-ground voltages at bus 7 during a line-to-line fault without fault impedance at bus 5 (ILNEM ↔ EMT)

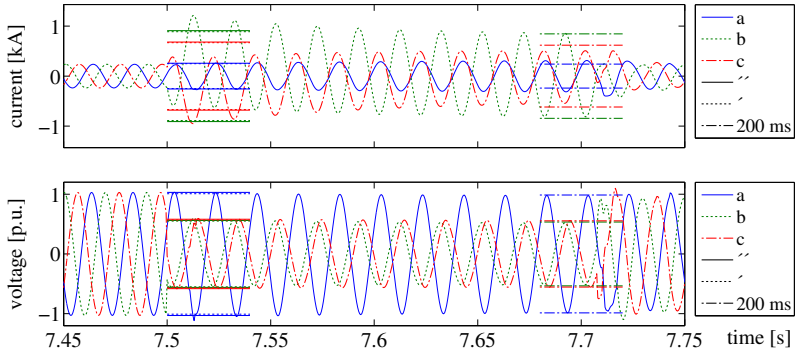


Figure 3.21: (Scaled) SG3 current and line-to-ground voltages at bus 9 during a line-to-line fault without fault impedance at bus 5 (ILNEM ↔ EMT)

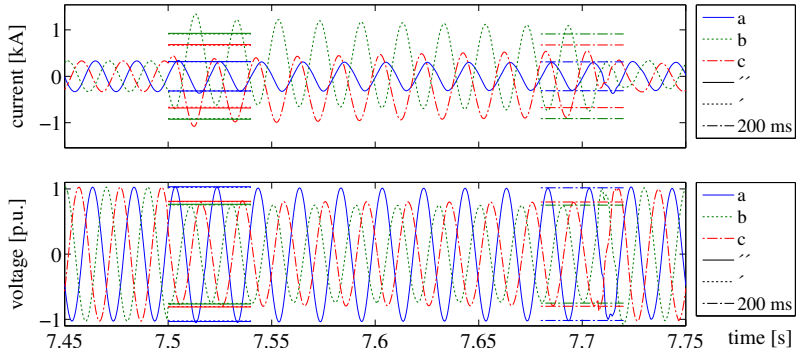


Figure 3.22: (Scaled) SG1 current and line-to-ground voltages at bus 4 during a distant line-to-line fault (ILNEM ↔ EMT)

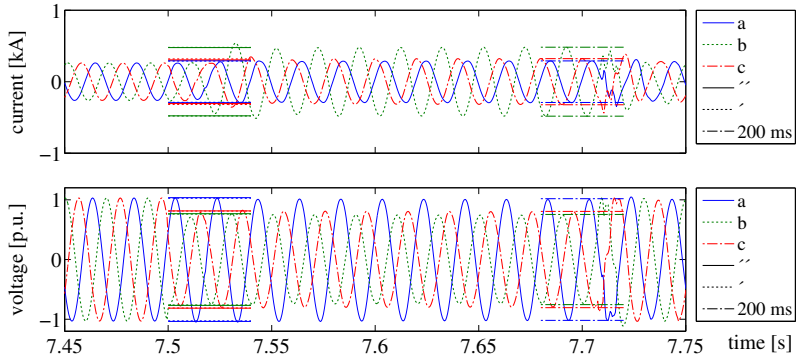


Figure 3.23: (Scaled) VSC current and line-to-ground voltages at bus 7 during a distant line-to-line fault (ILNEM ↔ EMT)

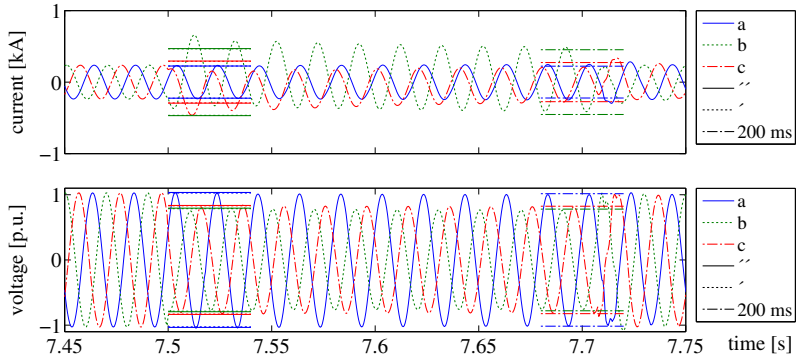


Figure 3.24: (Scaled) SG3 current and line-to-ground voltages at bus 9 during a distant line-to-line fault (ILNEM ↔ EMT)

3.4.4 Limitations of the ILNEM

The validation presented here demonstrates that the ILNEM calculation is able to model the fundamental frequency components of the currents and voltages in the system during both balanced and unbalanced faults. Of course, higher frequency behaviour and DC components cannot be represented in the calculations. Some papers [41–43] have suggested injecting harmonic distorted currents into unbalanced faults. These strategies cannot be evaluated with the ILNEM. However, these strategies seem to be unacceptable at a large scale as they would cause a large harmonic distortion in the grid when many CBDG units use these strategies during unbalanced faults, potentially triggering additional problems. Therefore, this work will not focus further on these types of strategies. A detailed discussion on alternative current injection strategies during unbalanced faults follows in chapter 5, section 5.2.

Furthermore, an important assumption of the ILNEM is that inertia is no issue or that the inertia challenge is taken care of already. When there are many CBDG units in the system and several conventional generators are taken out of service, the system inertia drops. This is not the topic of this dissertation and this dissertation assumes the inertia and frequency stabilisation issue during faults is evaluated with other models.

3.5 Conclusion

From the previous chapter, it is clear that the fault behaviour of CBDG units is determined by their control system. Therefore, any simulation method for fault studies, in grids with a high share of CBDG units, has to model the behaviour of the control system of the CBDG units. After a discussion of the alternative methods to represent CBDG units in fault studies, EMT simulations with AVMs are selected to model the detailed behaviour of the control system. Their accuracy, and the speed gains, are evaluated through a comparison with EMT simulations that use switched models. Afterwards, the Iterative Linear Network Equations Method (ILNEM) is selected as the simplest calculation technique that can model the fundamental frequency fault behaviour of the control system. This method is fine-tuned in this work, as a straightforward iteration does not guarantee convergence, and it is validated with EMT simulations.

ILNEM calculations are ideally suited to study the fault currents and voltages in networks with a high share of CBDG units, as other simulation methods are more computationally intensive. However, they can only by used after other verifications are performed. First, a verification of the detailed behaviour of

the control system should be done with EMT simulations and the transient stability of the system should be studied (e.g. with RMS simulations). After these verifications, or also for preliminary studies, the ILNEM calculations allow to study fault currents and fault voltages in the network without requiring the same detailed models of all network elements. The method will be used in the next chapters to evaluate different fault current contribution strategies of CBDG units during balanced and unbalanced faults.

Chapter 4

Fault Current Contribution Strategies during Balanced Faults

"Many hands make light work."
— John Heywood.

4.1 Introduction

In chapter 1, the effect of balanced faults was summarised. SGs inject large, (mainly) reactive currents into the fault and the resulting voltage drops over the (mainly) inductive grid result in a more local effect of the fault. When CBDG units replace conventional generation, and they don't inject reactive currents into the fault, the voltages in the grid will be smaller, resulting in a larger impact of the fault. In this chapter, the focus is entirely on this effect. Much work on the current injection and voltage support of DG units during balanced faults is already described in literature. Therefore, section 4.2 describes various aspects of this voltage support and gives an overview of the conclusions made in literature. The voltage support standards that are applied are also summarised. Other research on protection of distribution grids with a high share of DG units is treated briefly. Some control aspects treated in publication [50], to appear in IEEE Transactions on Energy Conversion, and in publication [114], made at

the IEEE PES General Meeting of 2015, are mentioned, although they are not the focus of this dissertation.

From the research on the protection of distribution grids, and the general voltage profile during faults, it is clear that a high short-circuit power has many advantages for the grid. Therefore, it is investigated whether CBDG units can contribute to the short-circuit power. The ILNEM developed in chapter 3 allows evaluating the trends of fault currents and fault voltages for different voltage support settings. Case studies, described in section 4.3, and presented at the IEEE PowerTech conference in 2015 [49], demonstrate that the flexibility of the CBDG units allows tuning the voltage support settings for the grid requirements, and that CBDG units can contribute to the short-circuit power.

4.2 Voltage Support during Balanced Faults

4.2.1 Voltage Support Standards during Balanced Faults

The FRT requirements for balanced faults were introduced in chapter 1. In addition, often voltage support is required during these faults. For this, both the German and Spanish grid codes require a reactive current injection in function of the voltage at the terminals of the CBDG unit [17, 23, 115–117]. The idea is to support the grid voltage during the fault, in a similar way the SGs do naturally. An example of a voltage support standard is given in Figure 4.1. This example is very similar to the previous German standard [116]. All quantities are expressed as positive sequence quantities as this chapter only treats balanced faults. There can be a DeadBand (DB), where no voltage support is required. There also is a static gain of the voltage support k_1, that can be varied between zero (no voltage support) and ten (maximum voltage support). This gain and the corresponding voltage measurement are defined at the Point of Common Coupling (PCC)[1], but can be converted to a gain and a voltage measurement for each individual unit. The Spanish standard is similar, but has variable gains, depending on the depth of the voltage dip [17, 115]. It should be noted that the reactive current is defined as additional reactive current injection and is thus related to the prefault values. The latest available German standard [117] has a similar approach, but no deadband and the static gain k_1 is between two and

[1]The PCC or network connection point is the point where the CBDG unit is connected to the grid. E.g. in case of a single WT, connected to a 10 kV MV grid, the PCC can be the 10 kV side of the transformer that connects the WT to the grid. In case of a WPP, consisting of several WTs with a small MV network that connects the WTs, the PCC can be the HV side of the step-up transformer that connects the small MV network with the WTs to the HV grid.

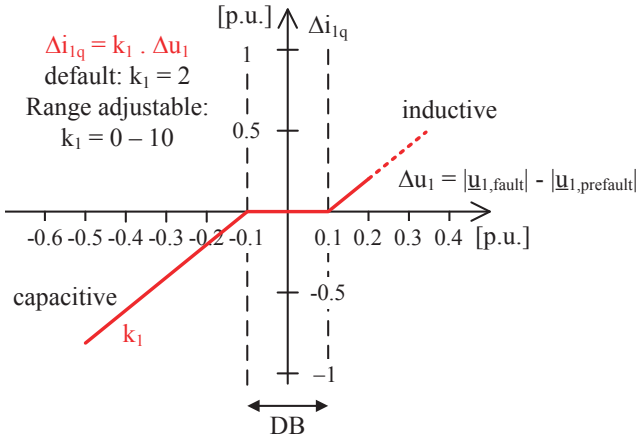


Figure 4.1: Example of a voltage support standard (generator sign convention)

six. The prefault voltage value is the 1-minute average value of the grid voltage before the fault detection. A CBDG unit has to be capable of injecting at least 100% of its rated current as reactive current during faults. The maximum rise and settling times are 30 ms and 60 ms respectively. In the UK, CBDG units have to inject the maximal reactive current during severe voltage dips due to network faults [23, 118], but no real gain is defined in the current grid code [118].

As the required current in these voltage support schemes often exceeds the rating of the CBDG unit, it is important to specify whether the active or reactive current has priority during faults. The German standard [116, 117] stipulates that the active current can be reduced when this is required.

This work does not treat DFIG WTs. However, in [119], it is shown that type 3 WTs can also follow the voltage support standard [116] with the specified rise and settling times. Therefore, this chapter is also valid for this type of DG, provided it uses the right control system. Some of the papers reported in the next sections use DFIGs, others use CBDG units.

Similarity between CBDG Voltage Support and SG Behaviour

Above, the similarity of the voltage support according to Figure 4.1 with the behaviour of a SG is mentioned. During balanced faults, only the positive sequence scheme is relevant. The equivalent model of a SG in the positive

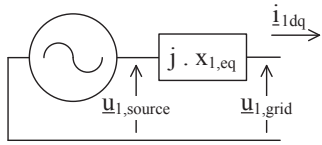


Figure 4.2: Positive sequence SG model with equivalent reactance $x_{1,\text{eq}}$

sequence scheme is described in section 3.4.1 and shown in Figure 4.2, when purely reactive impedances are assumed. For the subtransient case, the positive sequence reactance $x_{1,\text{eq}}$ equals $x_d^{''}$, for the transient case, $x_{1,\text{eq}}$ equals $x_d^{'}$.

Assume $x_{1,\text{eq}} = 0.5$ and the prefault values (the variables $\underline{u}_{1,\text{source}}$, $\underline{u}_{1,\text{grid}}$ and $\underline{i}_{1dq} = i_{1d} + j \cdot i_{1q}$ are indicated in Figure 4.2 and expressed in a reference frame aligned to the grid voltage):

$$\underline{u}_{1,\text{grid,prefault}} = 1 \qquad \underline{i}_{1dq,\text{prefault}} = 0.5 - 0.2 \cdot j \tag{4.1}$$

$$\Rightarrow \underline{u}_{1,\text{source}} = 1.1 + 0.25 \cdot j \tag{4.2}$$

All values are expressed in p.u.. As explained in appendix A.1, the generator sign convention is used in this dissertation, i.e. in a voltage oriented reference frame, a positive i_{1d} means active power is injected into the grid and a negative i_{1q} means the reactive power is capacitive.

When the grid voltage drops to 0.5 p.u., the resulting current is (assuming the source voltage is constant, as is the case in the SG model from Figure 3.9):

$$\underline{i}_{1dq,\text{fault}} = 0.5 - 1.2 \cdot j$$

and it is clear that

$$\begin{aligned} \Delta i_{1q} &= -1 \\ &= k_1 \cdot \Delta u_{1,\text{grid}} \end{aligned}$$

with $k_1 = \frac{1}{x_{1,\text{eq}}} = 2$.

This clarifies the similarity between the CBDG voltage support from Figure 4.1, with a fixed gain and without deadband, and the SG behaviour. Within its current limit, a CBDG unit with a gain k_1 of 2/3/4/5 thus has a comparable fault behaviour with a SG with an equivalent reactance of 0.5/0.33/0.25/0.2 p.u..

4.2.2 Different Aspects of the Voltage Support Current Injections

Considerable research has been performed on the effect of voltage support by CBDG units and in particular for WTs. A relevant selection of this research is discussed here.

Phase Angle of the Current Injection

Most voltage support standards require an additional reactive current injection as is discussed in section 4.2.1. In literature, the optimal current injection has been studied by taking the R/X ratio of the grid into account [120]. This dependence is also reported in [121, 122]. When the goal is to boost the voltage at the PCC of the CBDG unit, the optimal current injection, expressed in the generator sign convention, has an angle $\theta_{\mathrm{I}} = -\theta_{\mathrm{Z,tot}}$. This is under the assumption that $Z_{\mathrm{tot}} = |Z_{\mathrm{tot}}| \cdot e^{j \cdot \theta_{\mathrm{Z,tot}}} = R_{\mathrm{tot}} + j \cdot X_{\mathrm{tot}}$ is the impedance between the grid voltage and the PCC and that any (fault) impedance connected at the PCC has the same phase angle.

[120] also concludes that the voltage at the PCC can be boosted more if the short-circuit power of the grid is lower and that the effect of a certain current injection is higher if the residual voltage without voltage support is higher (i.e. for faults further away).

When a current with a certain phase angle θ_{I} is injected, this is of course different from the voltage support standard specified in Figure 4.1. In that case, the active current can be reduced if the current limit of the CBDG unit is exceeded. The voltage support standard also requires an additional reactive current injection. The advantage of this approach is of course that when the fault is cleared, the situation will be closer to the prefault situation. However, from a voltage boosting point of view, it is not the optimal current injection.

Limitations on the Current Injection

Already in [120], it is mentioned that the stability limit can impose a different current injection compared to the one obtained from the voltage support standard. A voltage dependent current limitation is suggested there. A very interesting work, that continues on the limitations of the current injections, is described in [122]. There, the active and reactive current transfer limits

between two buses are derived. The results[2] show the maximal amplitude of the current limit I_{lim}, when the angle of the current is θ_{I}, the impedance of the line between the buses equals $|Z| \cdot e^{j \cdot \theta_{\text{Z}}} = R + j \cdot X$, the sending bus 1 has a voltage $U_1 \cdot e^{j \cdot \theta_{\text{U1}}}$ and the receiving bus 2 has a voltage $U_2 \cdot e^{j \cdot 0}$:

$$\begin{aligned} 90^\circ - \theta_{\text{Z}} > \theta_{\text{I}} > 270^\circ - \theta_{\text{Z}} \qquad &\Rightarrow \qquad I_{\text{lim}} = \frac{U_2}{|Z| \cdot |\sin(\theta_{\text{Z}} + \theta_{\text{I}})|} \\ 270^\circ - \theta_{\text{Z}} \geq \theta_{\text{I}} \geq 90^\circ - \theta_{\text{Z}} \qquad &\Rightarrow \qquad I_{\text{lim}} = \frac{U_2}{|Z|} \end{aligned} \tag{4.3}$$

Although this is a theoretic case[3], it clarifies that, especially during deep voltage dips, not any current can be injected. When a pure (capacitive) reactive current is injected, the current is limited to $\frac{U_2}{R}$. It also clarifies that a current injection with angle $\theta_{\text{I}} = -\theta_{\text{Z}}$ is not limited (except of course by the value of the source U_1). When the grid is mainly inductive and the voltage dip is not very low, this current limit is usually above the current capacity of the CBDG unit and does not interfere with the voltage support strategy. It is also clear that the unlimited current transfer angle $\theta_{\text{I}} = -\theta_{\text{Z}}$ is the same as the angle that gives the maximal voltage boost according to [120], as is explained above.

It should be stressed that the active power injection during faults also has different functions: injecting more active power results in an easier FRT of the CBDG unit as the difference between the primary power generation and the power given to the grid decreases. However, this primary power generation depends on the operating point of the CBDG unit prior to the fault and, in general, during a balanced voltage dip, it is not possible to transmit the full power from the primary source to the grid. The active power is also connected to the frequency response of the grid and its inertia. [122] makes further analyses on the effect of the transfer limits on the loss of synchronism of WTs and suggests solutions to alter the current references during faults to avoid this loss of synchronism. These topics are not treated further in this dissertation, but are discussed extensively in literature. The evaluation requires an accurate load model during voltage dips and a detailed model of the grid inertia. However, the transfer limits will be taken into account in all simulations in this dissertation as only stable situations are reported. The discussion here also illustrates that certain design choices, e.g. the priority for active or reactive current, depend on multiple aspects.

[2] [122] uses a relatively unconventional sign convention of clockwise angles. The results are converted to the generator sign convention, similar to the previous section, and all angles are defined positive counter-clockwise.

[3] In real fault situations, there is no fixed receiving bus voltage or this voltage is not known by the sending bus (= the CBDG unit).

Influence of Voltage Support on the Transient Stability

In general, when the voltage is boosted, the transient stability is improved in the grid as the impact of the fault is reduced. [123] explicitly investigates the influence of the gain and the deadband of the voltage support on the transient stability of the network. From the results there, it is concluded that the deadband adversely affects the post fault transient performance. It is also concluded that a higher gain improves the transient stability. The same conclusion about the benefit of higher gains and the negative effect of the deadband on the post-fault voltage recovery is also made in [124,125]. [125] also compares the different options for active/reactive current priority and concludes that reducing the active current, to be able to inject more reactive current, has a positive effect, but it warns for applying this strategy in grids with a high R/X ratio. This is in line with the research on the phase angle of the current injection that is discussed above.

Other voltage support strategies are also investigated in [121,126]. In [121], the reactive current in function of the voltage dip, similar to Figure 4.1, is the best option from four different voltage support strategies (including a zero power mode and a maximum current strategy, similar to the UK grid code [118]). In [126], also the FRT requirements are linked with the voltage support strategy and the effect on the post-fault conditions, also for CBDG units connected to the LV grid.

From a transient stability point of view, there is thus a general consensus in literature that a proportional voltage support without deadband is the best voltage support option for CBDG units.

4.2.3 Influence of (the Voltage Support of) CBDG Units on the Power System Protection

One of the key questions when starting this dissertation was how DG units influence the protection of distribution networks (MV and LV). A literature review showed however that most of the theoretic problems concerning the integration of DG, e.g. blinding of protection or false tripping, are limited when SGs are integrated in typical European MV grids with relatively short feeder lengths [36,127]. In addition, many of the problems that arise, can be tackled with relatively simple, and local, solutions. One of the main conditions for this is that the short-circuit power, supplied by the HV grid, is sufficiently high. There are several papers in literature where protection issues are illustrated. However, a critical reflection on these publications often shows that unrealistic assumptions are made on the short-circuit power supplied by the HV grid.

Therefore, a case study in section 4.3 illustrates how the short-circuit power changes, depending on the voltage support settings of CBDG units. Whenever the short-circuit power does not change radically, protection problems remain relatively easy to tackle locally, like in [36]. In addition, CBDG units inject much smaller fault currents compared to SGs [66, 128, 129] and therefore, they will less likely impact the protection system. On the LV grid, many of these conclusions remain valid: whenever a large short-circuit power is delivered by the MV grid, little problems arise [130]. In addition, the longer clearing times at the lower voltage levels often result in a disconnection of the DG units as they are not required to have FRT for these long fault durations.[4]

Literature also mentions that CBDG units and Flexible AC Transmission Systems (FACTS) can have an adverse impact on the operation of distance relays [131, 132]. The main reason is that these devices cause interharmonics and subharmonics that influence the estimation of the fundamental frequency components used in the relays. Advanced filtering techniques can improve the performance of the relays [133]. In addition, the control of the CBDG unit can interfere with the fault detection. As was already mentioned, the voltage support standards require rise times of 30 ms and settling times of 60 ms. Compared to the instantaneous, natural response of SGs, this is relatively slow as some protection relays make decisions within this time frame. Therefore, the settings of the relays should take the response of these VSC units into account when they have an influence on the fault currents. For relays that have slower decision times, there should be no problems as the fault response of the VSC units is settled by then. Studying these issues requires detailed models of the relays and EMT simulations. This topic is out of the scope of this dissertation. However, it is identified as one of the issues that should be studied in future research.

4.2.4 Control Aspects of the Voltage Support

In chapter 2, the current controller of the GSC of a CBDG unit was explained in detail. Discussing the complete control system of the CBDG unit is outside the scope of this work, but some aspects related to the voltage support, are summarised below. These control aspects are discussed in two publications

[4] Examples of FRT requirements are given in section 1.1.2, see Figure 1.3. The reason why there are no FRT requirements for low voltages during long fault durations is that faults on the higher voltage levels normally have short clearing times. Faults on the lower voltage levels can have longer clearing times. However, a fault on a lower voltage level has a smaller impact (i.e. the voltage dip is only noticed on a small part of the grid) and the impact of losing generation in this part of the grid is much smaller than the impact of losing generation in a large part of the grid (which would be the case when there is no FRT for faults in the HV grid).

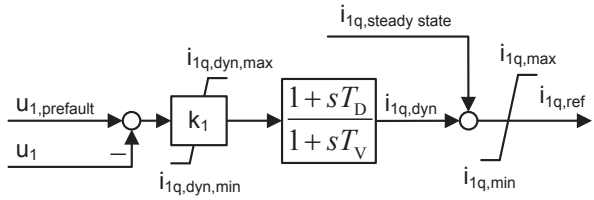


Figure 4.3: Outer positive sequence dynamic voltage control together with steady state reference

[50,114]. In [50], the control of type 4 WTs during unbalanced faults is discussed and chapter 5 will come back to these results. Some control aspects are also relevant for the control of CBDG units during balanced faults and these are treated here. In [114], the response of a hybrid AC-DC transmission system to balanced and unbalanced faults on the AC part of the network is discussed, including control aspects. As stated in chapter 1, the VSC of a HVDC connection also acts as a large CBDG unit and therefore these control aspects are also relevant.

Avoiding the Deadband in the Voltage Support

A voltage support standard, similar to Figure 4.1, requires that a current reference is generated and passed on to the current controller. In addition, the goal of the voltage support during balanced faults is an additional reactive current injection. Therefore, the control should not be active in steady state. One solution for this is applying a deadband. However, as is clear from the literature results above, the deadband has a negative impact on the transient stability of the power system. Therefore, in [50, 114] one possible control structure is given to avoid the deadband. This control structure is shown in Figure 4.3. The dynamic voltage support control is added to the steady state reference, which changes slowly. There are various control options for calculating the steady state reference, such as reactive power control, power factor control or voltage control. The prefault voltage is filtered with a time constant of 60 s, thus it is nearly constant during fault events. In the dynamic part, the voltage difference between the prefault and the fault voltage is multiplied with the gain k_1, corresponding with a proportional controller. The lead-lag compensator guarantees a fast but controlled response of this proportional control. Of course, the limits applied to this control depend on the active current reference and the priority that is given to active or reactive currents.

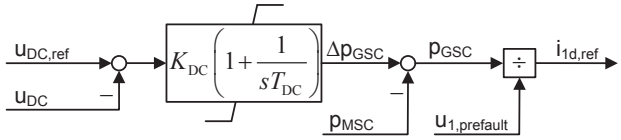


Figure 4.4: DC voltage control

Active Power Reference and Excess Active Power

In [50], some control aspects of the active current reference are discussed, specifically for type 4 WTs. In order to balance the power between the DC and AC side of the GSC, the outer power control loop, see Figure 4.4, consists of a DC voltage controller, a feed-forward term (active power of the MSC) and a division by the prefault grid voltage, which is filtered again with a large time constant. The output is the active current reference for the positive sequence current control.

The active current is in steady state prioritised in order to guarantee active power transfer through the converter. Under dynamic fault conditions, the positive sequence voltage drops and the active current reference increases. In addition, during faults, the priority can change to the reactive current for the voltage support, and then the active current has to be limited. Consequently, there is a power unbalance between the DC and AC side of the converter. The DC chopper with a braking resistor can be used to absorb the excess power in the DC link by converting it into heat. For HVDC, an alternative control, that varies the active power reference, is suggested in [114] to eliminate the need for a DC chopper.

It is clear that the choices of the priority for active or reactive current and maybe some optimisations to the phase angle of the injected current during voltage support, as discussed above, influence the limitations imposed to the active and the reactive current that can be injected during faults.

4.2.5 DFIG Balanced Fault Behaviour

As was already mentioned in section 4.2.1, when DFIGs follow the voltage support standards [116, 117], with the specified rise and settling times, their fault behaviour during balanced faults is similar to the fault behaviour of CBDG units. In this case, this chapter is also valid for DFIGs. Of course, the DC behaviour and specific DFIG aspects (e.g. crowbar actions) are not taken

into account. In addition, when the DFIGs' control systems do not follow the specified standards, the results are no longer valid for DFIGs.

4.3 Effect of CBDG Current Contribution on the Short-Circuit Power

As explained in the chapter 1, section 1.1.3, the short-circuit power S_{sc} is nothing more than a measure for the short-circuit currents in the system:

$$S_{\text{sc}} = \sqrt{3} \cdot U_{\text{nom,LL}} \cdot I_{\text{sc},3\varphi} \tag{4.4}$$

with $U_{\text{nom,LL}}$ the nominal line-to-line voltage and $I_{\text{sc},3\varphi}$ the three-phase short-circuit current at a point in the system.

In section 4.2.3, one of the main conclusions was that the impact of CBDG units on the protection system at the MV and LV level is limited if the short-circuit power coming from the higher voltages is sufficiently high. However, when centralised generation is replaced by DG, the short-circuit power also changes. The ILNEM developed in chapter 3 is ideally suited to evaluate how the short-circuit power changes when CBDG replaces conventional generation. Therefore, in publication [49], presented at the IEEE Powertech conference in 2015, a case study is described that assesses whether CBDG units connected to distribution grids can compensate (partially) for the short-circuit reduction that arises when conventional generation is taken off-line. This case study is discussed below. First, the test system and the scenarios are introduced. Afterwards, the results are presented and discussed.

4.3.1 System Description

The test system that is used is similar to the test system from section 3.4.3. It is also based on the WECC nine bus system with three synchronous generators (SG1-SG3) [113]. The line lengths are equal to the line lengths in section 3.4.3, but the loads are removed from the 230 kV voltage level and the system is extended with three subgrids that are identical with respect to their transformer and line parameters, Figure 4.5. All loads and CBDG units are connected to the 15 kV MV level of the subgrids and they are distributed equally over the Distribution Transformers (DTs). Both the Power Transformers (PTs) and the DTs in the subgrid have tap changers on the primary side to control the voltages at their secondary side. The generator, transformer and line data are given in appendix B: Table B.1, B.2 and B.3.

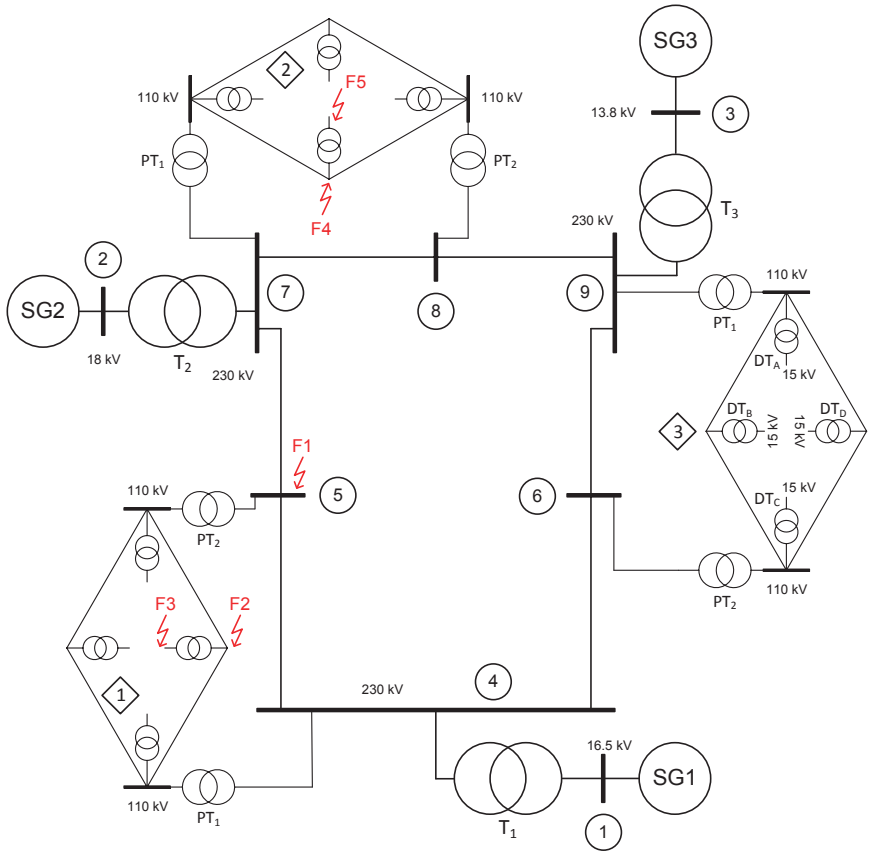


Figure 4.5: Test system: extension of WECC nine bus system
(Fault locations are indicated with a lightning symbol.)

Voltage Support and Calculation Details

For the calculations, the ILNEM described in chapter 3, section 3.4, is used. The new setpoints of the CBDG units are determined with:

$$\begin{aligned} I_{1d} &= I_{1d,\text{prefault}} \\ I_{1q} &= I_{1q,\text{prefault}} + \Delta I_{1q} \\ \Delta I_{1q} &= k_1 \cdot \Delta u_1 \cdot I_{\text{nom}} \end{aligned} \tag{4.5}$$

with I_{1d} the active current, I_{1q} the reactive current and I_{nom} the nominal current of the CBDG unit. The prefault values are determined by a load flow calculation.

Table 4.1: Load and CBDG data for configuration 1-3 / 4-6
(all values are given in the load sign convention)

Subgrid	**1**	**2**	**3**
P_{load} [MW]	125	90	100
Q_{load} [MVAr]	31.25	22.5	25
P_{CBDG} [MW]	0 / -25	-100 / -50	0 / -25
Q_{CBDG} [MVAr]	0 / -12.5	-50 / -25	0 / -12.5
$S_{CBDG,nom}$ [MVA]	0 / 192	192 / 192	0 / 192

Δu_1 is the difference of the per unit voltage at the terminals of the CBDG unit before and during the fault, as defined in Figure 4.1. A voltage deadband can be included to obtain a control as specified in [116], or excluded to obtain a control as specified in [117]. The voltage support is thus mainly determined by the gain k_1 and the voltage DeadBand (DB). If the total current exceeds the current limit I_{lim}, the current setpoints are scaled back. It is possible to scale down both active and reactive currents (as applied in the case studies below) or to give priority to the voltage support and first scale down the active current. It is also possible to disconnect the CBDG units at a certain voltage threshold, the disconnect voltage. In general, any current setpoint strategy that only depends on the voltage is possible with the ILNEM calculation.

As was mentioned in section 3.4.2, it is important to move gradually to the new setpoints when using the ILNEM. The convergence of the simulation is checked by monitoring the deviation of the CBDG units' injected currents with their setpoints. Large fluctuating deviations usually indicate that the stability limit is crossed. However, this only occurs for faults very close to the CBDG units when the grid is mainly inductive, as is explained in section 4.2.2. In this case study, this only occurs for faults at the CBDG units' terminals. As explained further on, in this situation the worst case short-circuit power is reported.

4.3.2 Scenarios

In order to compare the influence of the voltage support on the short-circuit power, 19 configurations of the test system of Figure 4.5 are considered. In the base case, there are no CBDG units in the subgrids and SG2 is connected to the system. In the other configurations, SG2 is out of service. The load and CBDG data is given in Table 4.1. In configuration 1, 2 and 3, there are CBDG units with the same total capacity (192 MVA) connected to subgrid 2

Table 4.2: Voltage support settings for the configurations

No.	deadband [p.u.]	disconnect voltage [p.u.]
1, 4	0.1	0.1
2, 5	0	0.1
3, 6	0.1	0

(equally distributed over the DTs) and in configuration 4, 5 and 6, there are CBDG units in all subgrids and the total capacity of CBDG units in the system is tripled (576 MVA). The settings of the voltage support are varied in the configurations. The deadband and disconnect voltage for the six configurations are given in Table 4.2. Additionally, the gain of the voltage support is varied between zero (no voltage support), two and five (a high gain, as a gain of six is the maximum gain according to the most recent German standard [117]). This results in 18 configurations with CBDG units. The CBDG units all have a short-term current limit of 120% I_{nom}.

Five faults are investigated (see Figure 4.5): a three-phase fault at bus 5 (230 kV, F1), at subgrids 1 and 2 on the primary side of $\mathrm{DT_B}$ (110 kV, F2 and F4) and at subgrids 1 and 2 on the secondary side of $\mathrm{DT_B}$ (15 kV, F3 and F5).

4.3.3 Results

Short-Circuit Calculations

In Figure 4.6, 4.7, 4.8, 4.9 and 4.10, the short-circuit power S_{sc} is compared with the short-circuit power of the base case for the 18 configurations (line equal to one is the reference for each figure).

From Figure 4.6, it can be concluded that the short-circuit power drops significantly when SG2 is disconnected from the system and the CBDG units do not provide voltage support. However, when they provide voltage support, the short-circuit power increases again. This leads to the conclusion that CBDG units connected at lower voltage levels can contribute to the short-circuit power at higher voltage levels. For scenarios 4 to 6, the loss of short-circuit power is even completely compensated. The difference between a modest gain of two and a high gain of five is relatively limited. The base case represents a relatively low short-circuit power scenario. However, additional calculations showed that when the size of the SGs is increased, and thus the base case short-circuit power is also increased, the same trend is noticed.

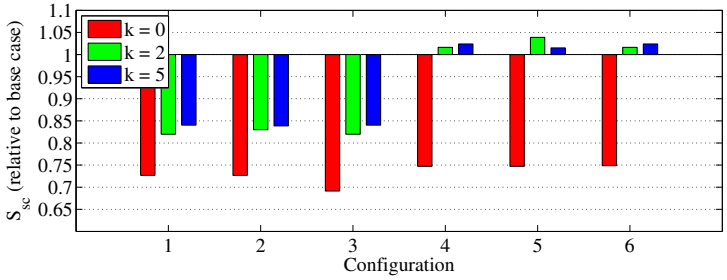


Figure 4.6: Short-circuit power at fault location F1
(base case: $I_{sc} = 3992\,A$, $S_{sc} = 1590\,MVA$)

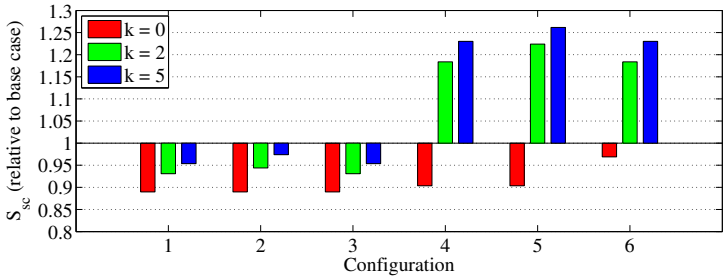


Figure 4.7: Short-circuit power at fault location F2
(base case: $I_{sc} = 3848\,A$, $S_{sc} = 733\,MVA$)

When the fault at location F2 is investigated (Figure 4.7), it can be seen that for scenarios 1-3 the trend in the short-circuit power is similar, but much less pronounced. In these scenarios, there are no CBDG units in subgrid 1, where the fault is located. Consequently, the fault currents are determined by the short-circuit power of the upper level and the impedances of the transformers. Because these transformers have a relatively high impedance, the short-circuit power changes less. This trend is repeated for the fault at location F3 (Figure 4.9). When the faults at location F4 and F5 are investigated (Figure 4.8 and 4.10), the same scenarios show an increase of the fault current when there is voltage support because the CBDG units in subgrid 2, where the fault is located, contribute to the short-circuit power locally.

For scenarios 4-6, the short-circuit powers at locations F2-F5 are higher because for these faults there are always local CBDG units in the subgrids and the short-circuit power at the 230 kV grid is higher as explained before.

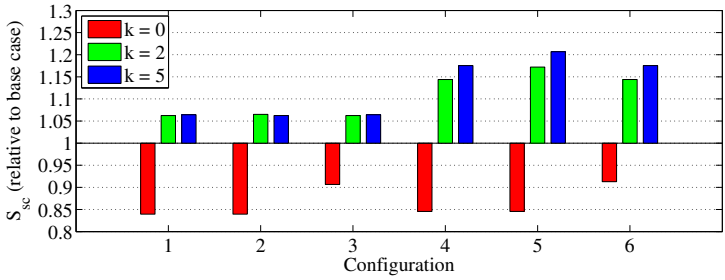


Figure 4.8: Short-circuit power at fault location F4
(base case: $I_{sc} = 3747\,A$, $S_{sc} = 714\,MVA$)

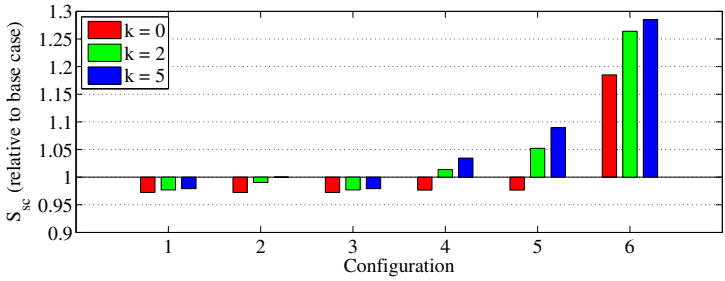


Figure 4.9: Short-circuit power at fault location F3
(base case: $I_{sc} = 8854\,A$, $S_{sc} = 230\,MVA$)

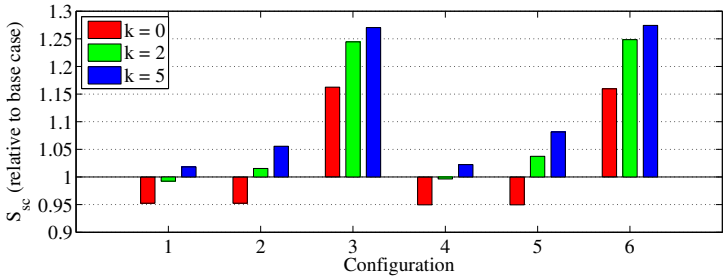


Figure 4.10: Short-circuit power at fault location F5
(base case: $I_{sc} = 8798\,A$, $S_{sc} = 229\,MVA$)

Influence of the Settings of the Voltage Support

When looking into more detail to the influence of the settings of the voltage support, it can be concluded that the deadband mainly has an (limited) influence on the short-circuit power. Only the CBDG units that have a limited voltage drop will inject more reactive current during the fault when there is no deadband. The CBDG units that experience a large voltage drop already inject their maximal current with the deadband.

It is clear that for the faults at MV level (F3 and F5), the disconnect voltage setting has a big influence. This is due to the fact that the CBDG units connected to one DT can contribute up to 57.6 MVA of short-circuit power, i.e. 120% of their nominal apparent power, and the base case only has a short-circuit power of 230 MVA. Whether the local CBDG units disconnect obviously influences the short-circuit currents significantly. Configuration 4 (the CBDG units from DT_B disconnect) and configuration 6 (no disconnection) illustrate these statements. It should be noted that the calculations for these faults represent the worst case scenario. The voltage between the rest of the grid and the CBDG unit equals zero. Mathematically, the link between the angle of the CBDG unit's current contribution and the other current contributions is lost. However, the angle of the current contribution is chosen to be the worst case angle, i.e. resulting in the highest total short-circuit current, and the magnitude is chosen to be the limit value of $120\%\, I_{\mathrm{nom}}$. For the scenarios without voltage support, this value is $100\%\, I_{\mathrm{nom}}$ as this is the worst case prefault value. For the faults at 110 kV level (F2 and F4), a similar approach was used, but the relative influence is smaller.

Additionally, the voltage during the fault is compared in Figure 4.11 and 4.12 for configuration 4 and 5, at two locations in the grid: at subgrid 1, MV side of DT_B, and at bus 6. Here, it is clear that the voltage support mainly boosts the voltage locally. For a fault at fault location F4, the higher gain of the voltage support and a smaller deadband clearly result in higher voltages.

These results prove that the influence of the CBDG units on the short-circuit power is highly dependent on the settings of the voltage support. This allows to tune the settings of the voltage support based on the requirements of the HV grid, but to take into account constraints in the short-circuit power of the local grid. When the short-circuit power, and thus the short-circuit current, is not close to the local limits, voltage support can be encouraged. However, for distribution grids that cannot handle the additional short-circuit power, setting the gain of the voltage support to zero can allow integrating additional CBDG units without the high cost of network reinforcements.

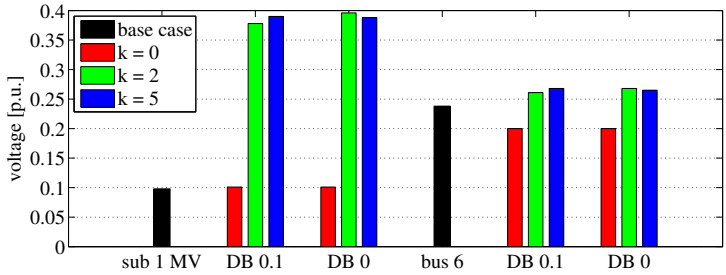


Figure 4.11: Voltage at subgrid 1, MV side of DT_B, and at bus 6 during a fault at location F1 (base case compared to configuration 4 and 5)

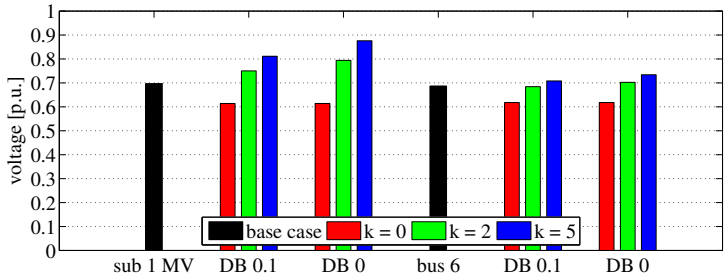


Figure 4.12: Voltage at subgrid 1, MV side of DT_B, and at bus 6 during a fault at location F4 (base case compared to configuration 4 and 5)

Additional Findings

It can be seen that when the CBDG units keep their prefault current setpoints, their effect can be negative. This is illustrated for a fault at location F1, Figure 4.6, where the short-circuit power in configuration 3 is lower than in configuration 1. A better option would be to at least reduce the current setpoints for such low voltages. For configuration 4, most CBDG units in subgrid 1 are just above the disconnection threshold, resulting in little difference with scenario 6.

The investigated cases assume an additional reactive current injection for the voltage support. The active current is determined by the prefault value and is reduced when the current capacity would be exceeded. As indicated by [120] and discussed in section 4.2.2, this is not the optimal current injection for maximal voltage support. However, in grids that are mainly inductive, it is a good approximation. This can also be seen in the results. Usually, the higher gain of the voltage support results in a higher short-circuit power. Only for fault F1 and configuration 5, the voltage support with gain two results in a

higher short-circuit power than the voltage support with gain five. In both cases, the CBDG units close to the fault inject their maximal current. However, the setpoint for the active current is reduced more when the gain equals five and apparently this current is less optimal than the current that is injected when the gain equals two.

All results are based on ILNEM calculations with the subtransient reactance for the SGs (subtransient calculations). Transient calculations were also performed, but these resulted in lower short-circuit power values, indicating that the lower contribution of the SGs was never overcompensated by a higher contribution of the CBDG units.

4.3.4 Discussion

Conclusions of the Case Study

It is clear that when CBDG units without voltage support replace conventional generation, the short-circuit power is reduced mostly on the highest voltage level and much less on the lower voltage levels. This is caused by the decoupling of the short-circuit power over the voltage levels, through the transformers. This is of course also the case in grids without DG units.

With voltage support, the short-circuit power is reduced less and in some cases the short-circuit power can even increase. This increase is mostly visible on the lower voltage levels that are closer to the CBDG units. Additional impedances between the CBDG and the fault decrease the contribution of the CBDG as they experience a smaller voltage dip for the same current injection. However, also CBDG units further away from the fault can contribute to the short-circuit power. When the short-circuit power drops, the voltage dips during faults increase and CBDG units will contribute more to the fault current. This way, CBDG units always limit the drop in short-circuit power when they provide voltage support. These conclusions are valid for all investigated settings of the voltage support. The exact impact of these settings, i.e. the gain, the deadband and the disconnect voltage, is of course network dependent, but the principles have been demonstrated: they have a bigger influence locally than for the higher voltage levels.

When the trend to more CBDG units and fewer SGs continues, applying voltage support for the CBDG units limits the drop in short-circuit power at the HV grid. As explained in section 1.1.3, a high short-circuit power has many positive effects. In addition, this means that the short-circuit currents at the lower voltage levels, supplied by the higher voltage levels, will not change radically. At

these lower voltage levels, the protection system relies on the magnitude of the fault currents and therefore, it is important that the short-circuit power does not drop too much. Changes to the protection system are then only required when the CBDG units influence the local protection system (e.g. blinding of the protection, false tripping), but as mentioned in section 4.2.3, this is usually not the case or the problems can be solved with local adaptations to the protection system. At the higher voltage levels, more advanced relays are often used and these relays do not only depend on the magnitude of the fault currents. This means that all protection systems (at the lower voltage levels) require little or no adaptations. When voltage support is not applied in scenarios with a high share of CBDG and little conventional generation, the short-circuit power is reduced, again mostly on the highest voltage levels, but also at the lower voltage levels. This may require a redesign of the grid protection systems at the lower voltage levels.

These findings allow to tune the settings of the voltage support based on the requirements of the HV grid (i.e. a sufficiently high short-circuit power), but to take into account constraints in the short-circuit power of the local grid (i.e. not exceeding the breaking capacity of the circuit breakers or the short-circuit withstand capability of the grid elements, as explained in section 1.1.3).

Limitations of the Case Study

The case study presented here has several limitations: e.g. the phase angle of the current injection is not optimised, LV units and the LV grid are not modelled. The grid is thus mainly inductive. Nevertheless, the concept of CBDG units connected to lower voltage levels, contributing to the short-circuit power at higher voltage levels is illustrated.

The research performed in [36], that is discussed in section 4.2.3, is more representative for European grids, where typically cable networks with relatively short feeder lengths are used for the MV and LV grids. These relatively short MV cables have lower impedances compared to typical MV overhead lines, e.g. used in North-American grids. For a typical European MV grid, this means that the short-circuit currents are high within the whole MV network if they are high at the MV side of the HV/MV distribution transformer. The protection systems of these grids are designed to take this into account: e.g. definite-time overcurrent relays are typically used in European MV grids, while inverse-time overcurrent relays are used together with reclosers in North-American MV grids [36]. Therefore, the conclusions on the protection system are more representative for European grids.

The limitations of the ILNEM also apply to this case study. It is not possible to study all system aspects with this simplified calculation method. For instance, based on this study, there are no objections to applying a high gain for the voltage support. However, the small signal stability of scenarios with a high gain should be verified with other simulations before concluding that this is a valid statement.

4.4 Conclusion

This chapter discussed the fault current contribution strategies during three-phase faults. It is clear from literature that voltage support by DG units has advantages for the transient stability of the power system. In the voltage support standards, there is a tendency to provide an additional reactive current during faults. Research has also shown that there are limitations to the current injections and that optimisations to the phase angle of the current injections are also possible. Due to the limited current capacity of CBDG units, the priority for active or reactive current has to be determined. It is also clear that not only the voltage support, but also other aspects such as loss of synchronism, grid frequency support, ... play a role in determining this priority.

Other research showed that the impact of CBDG units on the protection system of European MV and LV grids is limited when the short-circuit power supplied by the higher voltage levels is sufficiently high. Changes to the protection systems at these voltage levels are then only required when the CBDG units influence the local protection system, but this is usually not the case or the problems can be solved with local adaptations to the protection system. In this chapter, a case study shows that CBDG units connected at lower voltage levels can contribute to the short-circuit power at higher voltage levels when the CBDG units provide voltage support. This way, the CBDG units limit the drop in short-circuit power at the higher voltage levels when they replace conventional generation. This limits the impact of these scenarios on the protection system at the MV and LV level. Applying voltage support thus avoids a complete redesign of the protection systems at the lower voltage levels of typical European grids in scenarios with a high share of CBDG and little conventional generation. Locally, the voltage support of CBDG units can result in a (limited) increase of the short-circuit power. Therefore, this voltage support can be applied until the short-circuit power limits of the local grid, i.e. the breaking capacity of the circuit breakers and the short-circuit withstand capability of the grid elements, are reached.

Chapter 5

Fault Current Contribution Strategies during Unbalanced Faults

"CBDG units can have the best intentions, but offering the wrong help at the wrong time, can be worse than not helping at all."
— (inspired by) Tonya Hurley.

5.1 Introduction

In this chapter, several fault current contribution strategies during unbalanced faults are evaluated. First, section 5.2 gives an overview of all strategies suggested in literature. Strategies that only provide positive sequence voltage support (and block the negative sequence current), strategies that minimise the power oscillations experienced by the CBDG unit during unbalanced faults and finally, positive and negative sequence voltage support strategies, that inject both positive and negative sequence reactive currents during unbalanced faults, are discussed. The control aspects of these strategies are not treated in detail, but the conclusions from publication [50], to appear in IEEE Transactions on Energy Conversion, are given where appropriate.

The research in literature shows several effects of the different fault current contribution standards, but an evaluation of large scale integration of CBDG is missing. The framework developed in chapter 3 allows to evaluate this large scale integration. After selecting the most suitable strategies based on section 5.2 and publication [50], the effect of these strategies, including blocking or injecting negative sequence currents, are investigated during several unbalanced faults. First, a small test system is used in section 5.3 to allow for a theoretic explanation of the effects seen on fault currents, voltages and power transfers of the generation units. A case study on a larger test system confirms these trends in section 5.4. Finally, the conclusions of this chapter are summarised in section 5.5.

5.2 Alternative Current Injections during Unbalanced Faults

This section describes alternative current injections during unbalanced faults that are reported in literature. Conventional SGs inject both positive and negative sequence reactive currents into unbalanced faults. These currents increase the positive sequence voltage and decrease the negative sequence voltage, leading to more balanced voltages in the grid. The behaviour of CBDG units during grid faults on the other hand, is completely determined by their control system, as was demonstrated in chapter 2. The voltage rise during only positive sequence reactive current injection was illustrated in section 2.4.3 (Figure 2.22). It was also shown that there are no voltage rises, but that the voltages are more balanced when both positive and negative sequence reactive currents are injected (Figure 2.21).

Only recently, a first standard requiring negative sequence voltage support has become available [117]. Before this standard, no specific requirements concerning the injection of negative sequence currents were made. Therefore, the steady state blocking of the negative sequence currents usually remained active during unbalanced faults, leading to only positive sequence current injections. These strategies and their drawbacks are discussed first in section 5.2.1. Other researchers have suggested injecting unbalanced and even harmonic currents for improving the FRT behaviour of CBDG by limiting the power oscillations experienced by CBDG units during unbalanced faults. These strategies are summarised in section 5.2.2. Finally, the first standard concerning negative sequence voltage support is discussed in section 5.2.3.

In this section, the conclusions from publication [50], to appear in IEEE Transactions on Energy Conversion, are discussed together with other

conclusions from literature. In [50], the control of type 4 WTs during unbalanced faults is studied. Three different dynamic voltage control options, and thus three different current injection strategies, during unbalanced faults are discussed: 1) the only positive sequence voltage support with only a positive sequence reactive current injection and blocking of the negative sequence current; 2) the only positive sequence voltage support with limitation of the positive sequence reactive current injection and blocking of the negative sequence current; and 3) the positive and negative sequence voltage support with both a positive and a negative sequence reactive current injection. The first two strategies are discussed in section 5.2.1 and the third strategy in section 5.2.3.

5.2.1 Only Positive Sequence Current Injection (and Negative Sequence Current Blocking)

In steady state, CBDG units block negative sequence currents as they lead to an oscillation in the power transfer from the CBDG unit to the grid. Usually, this control remains active during faults [134]. This section shows that this approach boosts the voltages in the healthy phases and leads to symmetrical fault currents. However, when the positive sequence voltage support, and the positive sequence reactive current injection, is limited, the drawbacks of this strategy can be limited.

Effects of only Positive Sequence Voltage Support without Limitation

When the voltage support strategy discussed in chapter 4, section 4.2.1, is applied during unbalanced faults, an additional positive sequence reactive current injection is required, as the positive sequence voltage drops during most unbalanced faults (e.g. single-line-to-ground or line-to-line fault). When the gain of the voltage support according to Figure 4.1 is relatively high, large additional reactive currents are required during an unbalanced fault. E.g. a gain $k_1 = 4$ and a fault with a positive sequence voltage drop $\Delta u_{1,\mathrm{grid}} = -0.25\,\mathrm{p.u.}$ requires an additional reactive current $\Delta i_{1q} = k_1 \cdot \Delta u_{1,\mathrm{grid}} = -1\,\mathrm{p.u.}$. Here, the only positive sequence voltage support without limitation means that the injected positive sequence current is determined by this voltage support and is not limited by other constraints, except of course the current rating of the converter. The additional reactive current injection boosts the positive sequence voltage. However, unlike for balanced faults, there are still negative and/or zero sequence voltages in the system. It is possible that the line-to-ground or line-to-line voltages in the system become higher than 1 p.u. and there are thus overvoltages in the system. Conventional SGs always boost the positive

sequence voltage during unbalanced faults, but they also reduce the negative sequence voltage at the same time so they don't cause additional overvoltages during unbalanced faults[1].

These theoretic considerations are confirmed in publication [50] and by several other researchers [122, 134–136]. In [122, 134], several unbalanced faults are studied. The fault is located on a transmission line that connects a WPP, i.e. a collection of several WTs, to the rest of the grid. The only positive sequence current injection of the WTs leads to the boosting of the positive sequence voltage. As there is no negative sequence current injection, the negative sequence voltage at the fault location propagates to the WPP, leading to overvoltages in the healthy phases. The coupling of the sequence schemes at the fault location is also specifically mentioned. A comparison with a SG with the same nominal power as the WPP is made and in that case there are no overvoltages.

Papers [135, 136] focus more on the control of CBDG, but indicate the same trend when an unbalanced fault occurs on the line connecting a CBDG unit with the grid and the CBDG unit only injects positive sequence currents into the fault.

Finally, publication [50] considers a meshed system, similar to the WECC nine bus system and Figure 3.12, where a WPP is connected to bus 2. In this study, realistic DC bus voltage levels of the individual WTs are considered. The study focuses on line-to-line faults as these lead to the highest negative sequence voltage impact on the WTs. When only positive sequence currents are injected, the voltages in the healthy phases are boosted. Additionally, the control of the WTs is partially lost because there is overmodulation and saturation in the control because of the limited DC bus voltage level. The voltages generated by the converter, and thus the currents of the WTs, are distorted. In addition, the currents are higher than the current limit set by the control system. If the DC bus voltage would be higher, there would be no saturation in the control, but the voltage increase in the healthy phase would even be larger. Increasing the DC bus voltage would however require changing the converter design specifically for the positive sequence current injection during unbalanced faults and would result in higher costs.

It must be noted that, while voltage support standards require that a CBDG unit can inject a reactive current equal to 100% of the rated current for balanced faults, this requirement drops to 40% for unbalanced faults [116]. However,

[1]Depending on the grid impedances, some unbalanced faults (e.g. single-line-to-ground faults) naturally cause overvoltages in the system. However, SGs do not reinforce these overvoltages. CBDG units that only inject positive sequence reactive currents do reinforce these overvoltages. In addition, on the higher voltage levels the grid impedances are designed in a way that there will only be limited overvoltages during unbalanced faults.

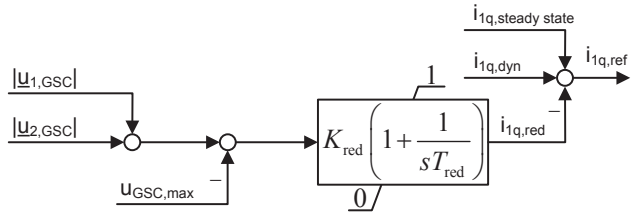


Figure 5.1: Control for limitation of the positive sequence reactive current

the standard does not really limit the positive sequence current injection. The next section discusses an intelligent limitation of the positive sequence current injection.

Only Positive Sequence Voltage Support with Limitation

An obvious extension of the control is to include a limitation on the positive sequence current injection, based on the voltage that is generated by the CBDG unit. This control was suggested in publication [50] and is shown in Figure 5.1. The reactive current that is injected is dynamically reduced when overmodulation in the control occurs. As can be seen in Figure 5.1, the positive and negative sequence voltage are added to check if the sum is larger than the maximum voltage that can be generated by the converter. When this is the case, the reduction term $i_{1q,\mathrm{red}}$ reduces the term of the dynamic voltage support. The negative sequence voltage that the converter has to generate is the negative sequence voltage at the terminals of the converter, in order to block the negative sequence currents. The detailed simulations in [50] show that only at the beginning of the fault, the voltage increase is similar to the positive sequence voltage support without limitation described previously. Afterwards, the voltage increase is limited by the control system. The CBDG unit remains controllable and the currents remain below their limits. This research leads to the conclusion that an only positive sequence voltage support without limitation is not a good strategy, but that the limited version is a valid option.

In this dissertation, the only positive sequence voltage support will always refer to this limited version of the positive sequence voltage support. It is never a good idea to deliberately control a CBDG unit by using overmodulation and probably the manufacturers of commercial CBDG units use a similar method to avoid this overmodulation. The only positive sequence voltage support (with limitation) will be compared with the alternative options further on in section 5.3 and 5.4.

5.2.2 Injection Strategies that Limit the CBDG's Power Oscillation

One of the advantages of a three-phase power system, is that under balanced conditions, there is constant power flow when the power flows in the three phases are added [137]. Consequently, SGs, IGs, CBDG units, ... operating under balanced conditions do not experience power ripples[2]. However, when the voltage is unbalanced or when unbalanced currents are injected by the generator, there are power ripples. Several publications in literature focus on limiting the power oscillations experienced by CBDG units during unbalanced faults. There are two major approaches for this: approaches that allow non-sinusoidal current injections by the CBDG unit and approaches that only allow sinusoidal (i.e. fundamental frequency positive and negative sequence) currents. The primary goal of these strategies is thus reducing the stress on the CBDG units and not necessarily supporting the grid voltage.

Harmonic Injections

A series of papers considers the instantaneous power theories to derive current injections that limit the power oscillations [41–45]. These papers start from:

$$p(t) = u_a(t) \cdot i_a(t) + u_b(t) \cdot i_b(t) + u_c(t) \cdot i_c(t) \tag{5.1}$$

to derive current references for CBDG units that guarantee a constant power. These current references are not sinusoidal. Several restrictions are added, e.g. no active power transfer in the negative sequence, to obtain alternative strategies. Then the restriction is added that the currents have to be sinusoidal. These current injection strategies are discussed in the next part. Finally, the only positive sequence current injection is mentioned, which is of course similar to the one discussed in section 5.2.1.

The harmonic injections are out of the scope of this dissertation as mentioned in section 1.2. The more recent papers [44, 45], from the same authors as papers [41–43], also focus on the sinusoidal current injections and [45] even warns for the drawbacks of non-sinusoidal currents: they impose high dynamic requirements to the current controller and they increase the voltage distortion at the PCC. Therefore, these harmonic injections are most likely unacceptable for the grid when they are applied on a large scale.

[2]Directly coupled generators therefore do not experience torque ripples on their axes.

Sinusoidal Positive and Negative Sequence Current Injection

Sinusoidal current injections, including negative sequence currents, are already suggested in [41–45]. In addition, several other papers suggest similar strategies [51,53,68,138–140]. They also consider the power transfer (5.1) and try to limit the power oscillations experienced by the CBDG units during unbalanced faults, but only fundamental frequency positive and negative sequence current injections are considered. Appendix A.3 details this instantaneous power transfer and the interpretation of Aredes [17,141] where the variable frequency p components represent a power exchange in and out of the system, while the q components indicate a power exchange between the phases. Equation (A.4) is repeated here for convenience:

$$\underline{s} = \underline{u}^{\angle 0} \cdot \underline{i}^{*\angle 0} \tag{A.4a}$$

$$= p + j \cdot q$$

$$p = p_0 + p_{c2} \cdot cos(2\omega t) + p_{s2} \cdot sin(2\omega t) \tag{A.4b}$$

$$q = q_0 + q_{c2} \cdot cos(2\omega t) + q_{s2} \cdot sin(2\omega t) \tag{A.4c}$$

The relation with the phasor values is given in (A.5).

It is common to try to minimise the variable p components to limit power ripples for the sources, as the q components do not influence the power ripple for the source (e.g. DC bus of converter, shaft of turbine) and the four fundamental frequency currents ($i_{1d}, i_{1q}, i_{2d}, i_{2q}$) only allow to control four of the six power components ($p_0, p_{c2}, p_{s2}, q_0, q_{c2}, q_{s2}$) [51,59,139]. This leads to current references that follow directly from the system voltages and include in general both positive and negative sequence active and reactive currents and thus unbalanced current injections. Some papers include the filter impedance to guarantee that the converter has no power oscillations compared to the CBDG unit as a whole [51, 139]. However, all these papers consider a CBDG unit connected to an infinite grid that can absorb or supply the active power in both the positive and negative sequence. In reality, the negative sequence active power has to be consumed by loads or transferred over the fault conditions to positive sequence active power. In addition, these papers do not evaluate what level of power oscillations of the CBDG units during unbalanced faults can be tolerated. This is identified as a topic that needs further research before considering these strategies that do not take the grid into account. The next section also describes a similar fault current injection strategy that applies a zero negative sequence active current reference and limits the power oscillations of the CBDG units with this additional boundary condition.

5.2.3 Positive and Negative Sequence Voltage Support

While the previous set of strategies focused completely on the CBDG units, the next set of strategies focuses more on the voltage support of the grid. First, an overview of a positive and negative sequence voltage support standard is given. Afterwards, an alternative positive and negative sequence reactive current injection strategy is discussed. The similarity between the positive and negative sequence voltage support and the behaviour of a SG is also clarified.

As opposed to the previous strategies, discussed in section 5.2.2, the positive and negative sequence voltage support strategy described in this section does not focus on the power oscillations of the CBDG units. This might have consequences for the FRT of the CBDG units. During balanced faults close to the CBDG unit's terminals, it is impossible to transfer the rated active power, as the voltage is much lower and the current capability of the converter is limited. Therefore, CBDG units have to cope with this excess power to fulfil the FRT requirements (e.g. through a DC chopper [51]). During unbalanced faults, the excess power will be smaller and will not cause additional FRT issues. The power oscillations do have to be taken into account in the design of the CBDG units, during the time prescribed by the FRT requirements. These power oscillations will be evaluated after this discussion in the case studies from section 5.3 and 5.4.

First Standard Requiring Positive and Negative Sequence Voltage Support

The positive and negative sequence current injections of the CBDG units are defined in this work as:

$$\underline{i}_{1dq} = i_{1d} + j \cdot i_{1q} \tag{5.3a}$$

$$\underline{i}_{2dq} = i_{2d} + j \cdot i_{2q} \tag{5.3b}$$

where both the positive and negative sequence components each have their own dq reference frame, aligned with the rotating positive/negative sequence voltage phasor ($u_{1d} = |\underline{u}_1|$ and $u_{2d} = |\underline{u}_2|$, cf. Figure 2.3 and 2.8). The small letters are p.u. values. To obtain the real current, the p.u. values are multiplied with the nominal current of the CBDG unit I_{nom}.

Figure 5.2 shows the most recent German voltage support standard VDE-AR-N 4120 [117]. This voltage support is defined by injecting a current (expressed in the generator sign convention):

$$i_{1d} = i_{1d,\text{prefault}} \qquad i_{1q} = i_{1q,\text{prefault}} + k_1 \cdot \Delta u_1 \tag{5.4a}$$

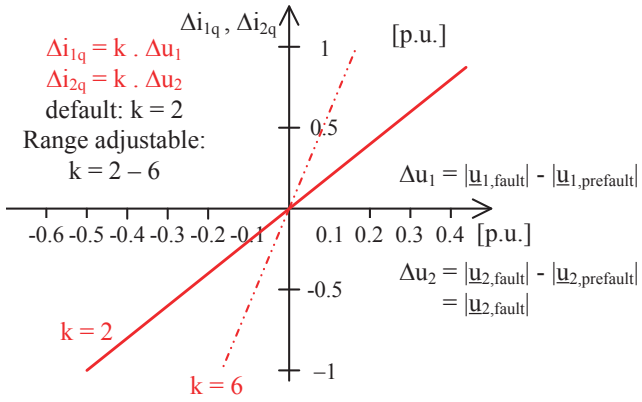


Figure 5.2: Example of a standard requiring positive and negative sequence voltage support [117] (generator sign convention)

$$i_{2d} = 0 \qquad i_{2q} = k_2 \cdot \Delta u_2 \tag{5.4b}$$

$$k_1 = k_2 = k \tag{5.4c}$$

It is currently the only voltage support standard requiring negative sequence voltage support. Some interesting choices were made. The gain in the positive and negative sequence is the same, although in general different gains k_1 and k_2 could be chosen. This gain and the voltage measurement are defined at the PCC, similar to section 4.2.1, but can be converted to a gain and a voltage measurement for each individual unit. The standard also mentions explicitly that CBDG units have to be capable to inject a total reactive current of 100% of the rated current and that, in case of current limitation, the active current can be reduced, but that equal priority to the positive and negative sequence current has to be given. There is no deadband, both in the positive and negative sequence. For low negative sequence voltages, this is a challenge as already indicated in section 2.4.1.

Although this standard was not available during most of the research period for this dissertation, a draft version [142] was available. The main difference between this draft version and the final version [117] is that a small deadband ($\pm 2.5\%$) is foreseen in the draft version. In [117], there is no deadband, but there are tolerance curves. With these tolerance curves, manufacturers can still implement a small deadband, but it is not required to implement a deadband. The voltage support only starts when there is a voltage jump or when the voltages are outside the 90% - 110% U_{nom} band. However, in [142] this voltage

jump is specified as being larger than 2.5%, but in [117] no specification of the size of the voltage jump is given.

In publication [50], this draft standard is investigated and compared to the only positive sequence voltage support. The deadband assumed there is 5%, as in [47] and section 2.4.1, this was derived to be a good deadband to obtain a stable estimation of the negative sequence phase angle. Lowering this deadband requires a further optimisation of the control system. In [50], the simulation results for a line-to-line fault show that there is no voltage increase in the healthy phase (the positive sequence voltage is increased and the negative sequence voltage is reduced), that the currents are controlled quite fast (approximately 30 ms) and that the currents don't exceed the current limit. The fault response is more similar to the response of a SG, with higher currents in the faulted phases than in the healthy phase. The priority for the reactive current in positive and negative sequence reduces the current capability for the active current in the positive sequence. Hence, the active current is limited to zero during the fault and is ramped up rapidly after voltage recovery, guaranteeing the active power balance in the meshed test system. In the case of only positive sequence voltage support, the required reduction of the positive sequence active current is clearly smaller.

Similar conclusions were made in [122,134], where a similar positive and negative sequence voltage support strategy is tested and compared with only positive sequence voltage support on a simpler test system. In [67], the effect of positive and negative sequence voltage support on the protection system is compared with a scenario where all negative sequence currents are blocked. The study is made on a small test network with one or two CBDG units. It is seen that the line-to-line fault currents are reduced to the level of load currents, or even to zero, when all sources in the system block the negative sequence current.

In conclusion, the effect of this positive and negative sequence voltage support is that the positive sequence voltage is increased due to a capacitive positive sequence reactive current injection, and the negative sequence voltage is decreased due to an inductive negative sequence reactive current injection. This balances the voltages and results in a CBDG's fault response that resembles more the fault response of a SG. The additional positive/negative sequence reactive current is determined by the positive/negative sequence voltage change.

Alternative Positive and Negative Sequence Reactive Current Injection Strategy

Regardless of the voltage support standard, another strategy is suggested in [135]. The positive and negative sequence reactive current references are defined

proportional to the positive and negative sequence voltage:

$$i_{1d} = i_{1d,\text{prefault}} \qquad i_{1q} = -c^{+} \cdot k_c \cdot u_{1d} \tag{5.5a}$$

$$i_{2d} = 0 \qquad i_{2q} = c^{-} \cdot k_c \cdot u_{2d} \tag{5.5b}$$

$$c^{-} = 1 - c^{+} \qquad c^{+} \in [0, 1] \tag{5.5c}$$

leading to a capacitive positive sequence reactive current and an inductive negative sequence reactive current injection. Varying k_c is similar to varying k in (5.4): a more sensitive voltage support, with higher current injections, is obtained. By varying c^{+}, a flexible voltage support is obtained. Taking $c^{+} = c^{-} = 0.5$, leads to a minimisation of the oscillating power for this strategy. This strategy is then very similar to the strategies discussed in [51,53,68,138–140] and in section 5.2.2. The main difference is that in [135], no active power is transferred in the negative sequence and that the power oscillations are reduced, but not avoided. The strategies are the same when no active power is transferred by the CBDG units.

The difference with the current injections according to the standard [117] is that in [135], the total reactive current injections are proportional to the total positive and negative sequence voltage (5.5), while in [117], the additional reactive current injections are proportional to the positive and negative sequence voltage change (5.4). As the currents are not defined as additional current injections, it is unclear how this strategy will affect the system after fault clearing and how the transients between this strategy and the normal operation should look like. It is therefore not considered as a suitable strategy.

However, the current injection according to [135] can be seen as a compromise between the only positive sequence voltage support and the postive and negative sequence voltage support. It will inject a smaller negative sequence current than the positive sequence current for most faults (usually $u_2 \leq u_1$, except at the location of a line-to-line fault $u_2 = u_1$). In section 5.3, this strategy (5.5) is investigated further and it is compared to strategy (5.4).

Similarity between the Positive and Negative Sequence Voltage Support Standard and the Behaviour of a SG

Conventional SGs contribute with an inherent short-circuit current consisting of positive and negative sequence to unbalanced grid faults. Here, it is shown that the fault response of a CBDG unit, that provides positive and negative sequence voltage support according to (5.4), is similar to the fault response of a SG. The similarity during balanced faults is already illustrated in section 4.2.1.

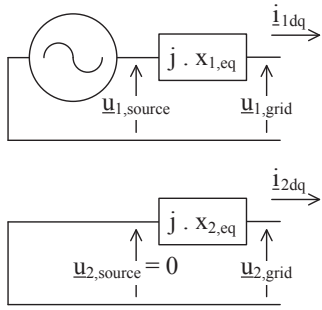


Figure 5.3: SG model with equivalent reactances $x_{1,\mathrm{eq}}$ and $x_{2,\mathrm{eq}}$

The equivalent model of a SG is described in section 3.4.1 and shown in Figure 5.3. When the subtransient case is considered, the positive sequence reactance $x_{1,\mathrm{eq}}$ equals x_d'' and the negative sequence reactance $x_{2,\mathrm{eq}}$ is about the same when the subtransient saliency is small (neglecting resistive parts). The same prefault conditions as in section 4.2.1 (4.1) are considered (there are no negative sequence voltages and currents in the prefault case):

$$\underline{u}_{1,\mathrm{grid,prefault}} = 1 \qquad \underline{i}_{1dq,\mathrm{prefault}} = 0.5 - 0.2 \cdot j$$

$$\Rightarrow \underline{u}_{1,\mathrm{source}} = 1.1 + 0.25 \cdot j$$

where all values are expressed in p.u.. Assume $k = 2$ and $x_{1,\mathrm{eq}} = x_{2,\mathrm{eq}} = \frac{1}{k} = 0.5$. When the positive sequence grid voltage $\underline{u}_{1,\mathrm{grid}}$ drops to 0.75 p.u. and the negative sequence grid voltage $\underline{u}_{2,\mathrm{grid}}$ rises to 0.25 p.u., the resulting current is (assuming the source voltage is constant and with the positive (negative) sequence variables expressed in a reference frame aligned to the positive (negative) sequence grid voltage):

$$\underline{i}_{1dq,\mathrm{fault}} = 0.5 - 0.7 \cdot j \qquad \underline{i}_{2dq,\mathrm{fault}} = 0.5 \cdot j$$

and it is clear that

$$\Delta i_{1q} = -0.5 \qquad \Delta i_{2q} = 0.5$$

$$= k \cdot \Delta u_{1,\mathrm{grid}} \qquad = k \cdot \Delta u_{2,\mathrm{grid}}$$

Thus the fault behaviour of a CBDG unit with voltage support according to (5.4) is similar to the subtransient fault behaviour of a SG, within the current limits of the CBDG unit and when the gain of the voltage support k is chosen correctly.

5.2.4 DFIG Unbalanced Fault Behaviour

Although the response of DFIGs is not treated in this dissertation, it is important to stress that a DFIG is (partly) directly connected to the grid (through the IG) and also has a power electronic interface. IGs naturally provide a negative sequence current into unbalanced faults and [143] points to the fact that this is also valid for DFIGs. This natural response is determined by the generator's reactances and is thus not controlled. The negative sequence current can be controlled due to the converter in the DFIG, but the controllability is limited by the converter rating. Therefore, [143] recommends to have no specific lower boundary for the negative sequence current contribution of a DFIG during unbalanced faults. A detailed study on the capability and the limitations of the negative sequence control for DFIGs is given in [39, 144–146]. Reference [38] gives detailed simulations of the response of a DFIG to unbalanced faults, including negative sequence control or with only the natural negative sequence response. The natural response shows a higher negative sequence reactive current than the positive sequence reactive current. With the negative sequence control, the difference between both is smaller, but the DFIG still delivers more negative sequence current than prescribed by (5.4), which is in line with the conclusions from [143]. Therefore, the studies performed in the next sections do not apply for DFIGs. On the other hand, it is also clear that in networks with both CBDG units and DFIGs, the DFIGs will supply more negative sequence reactive currents. This will decrease the negative sequence grid voltages and, as a consequence, the CBDG units will provide relatively more positive sequence reactive currents.

5.3 Effect of Blocking versus Injecting Negative Sequence Current - Theoretical Considerations in a Small Test System

In this section, a small test system is introduced to allow for a thorough analysis of the differences between different current injection strategies during unbalanced faults. Three strategies are investigated: (1) only positive sequence voltage support with negative sequence current blocking, (2) positive and negative sequence voltage support according to (5.4) and (3) the alternative positive and negative sequence reactive current injection strategy (5.5). First, the test system and the scenarios are introduced. Then the calculation method, based on the ILNEM, is explained. Afterwards, line-to-line, single-line-to-ground and two-lines-to-ground faults are analysed and finally, the results are interpreted.

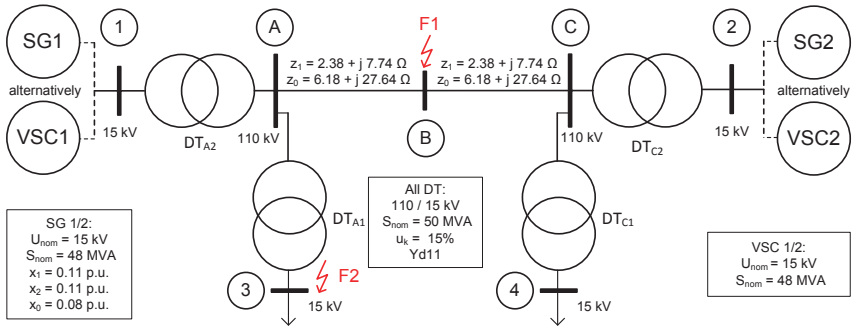


Figure 5.4: Small test system with two sources

5.3.1 System Description

In this first case study, a small test system with two sources is investigated. All system data is given in Figure 5.4. The load at bus 3 and 4 is 10 MW and 2.5 MVAr (inductive). The VSC units have a short-term overload capability of 120%. The source at bus 1 and bus 2 is alternatively a SG or a CBDG unit (a VSC) in the different scenarios that are explained below.

For the faults including ground, the earthing system is important, as it has a large influence on the zero sequence impedances. The starpoint of the primary side of DT_{A1} and DT_{C1} is earthed and the zero sequence impedance voltage u_{k0} is considered equal to the positive sequence impedance voltage u_k. The other DTs are not earthed. On the secondary side of DT_{A1} and DT_{C1}, an earthing transformer, that gives a theoretic single-line-to-ground fault of 1000 A, is connected[3].

5.3.2 Scenarios

The investigated scenarios are listed in Table 5.1. As a base scenario (no. 1), both sources are SGs. In scenarios 2-3-6, SG1 is replaced by VSC1, a converter based source. In scenarios 4-5, both SG1 and SG2 are replaced by VSC1 and VSC2 to obtain a system with only CBDG units[4]. The VSC sources will either

[3]This means the earthing transformer has a zero sequence impedance of 26 Ω. The single-line-to-ground fault is a bit smaller than 1000 A as there is also a positive and negative sequence impedance in the system.

[4]In the ILNEM calculations, the frequency is inherently fixed. In reality, these scenarios require a frequency / (virtual) inertia control to keep the frequency within acceptable limits. The case study thus assumes that such a control is available and implemented.

Table 5.1: Scenarios for the small test system

No.	Sources	Neg. seq. strategy
1	SG1, SG2	/
2	VSC1, SG2	block
3	VSC1, SG2	(5.4)
4	VSC1, VSC2	block
5	VSC1, VSC2	(5.4)
6	VSC1, SG2	(5.5)

block the negative sequence current (scenarios 2-4) or inject negative sequence reactive current according to (5.4) (scenarios 3-5). The gain of the voltage support according to (5.4), k_1, is 6.67 p.u., before the transformer (including the transformer impedance this becomes 3.4 p.u.). The gain k_2 is either zero (scenarios 2-4) or equal to k_1 (scenarios 3-5). Scenario 3 and 6 are similar, but in scenario 6, the current injection according to (5.5) is applied with $c^+ = c^-$ to minimise the power oscillations of the CBDG unit. This scenario is discussed at the end of section 5.3.4 below.

The fault locations F1 and F2 are indicated in Figure 5.4. First, line-to-line faults are discussed as these faults result in the highest negative sequence voltages and the difference between the injection and the blocking of negative sequence currents by the CBDG units is the largest for these faults. Afterwards, single-line-to-ground and two-lines-to-ground faults are also investigated. Although these faults are highly dependent on the zero sequence impedances (i.e. the earthing system of the network), the effect of the negative sequence current blocking or injection will be clear.

5.3.3 Calculation Method and Description in Symmetrical Components

For this study, the ILNEM calculation, explained in chapter 3, is used. However, when the CBDG units give full priority to the reactive currents and reduce their active power output during faults, the active power has to be delivered by the remaining SG, if there is one in the system. This can lead to an overload of the SG and an unrealistic calculation result. In reality, when the share of CBDG units is that high, they will have to contribute to the frequency regulation of the network and also contribute some active power. Therefore, the simulations use the current controlled voltage source model of the CBDG units. Figure 5.5

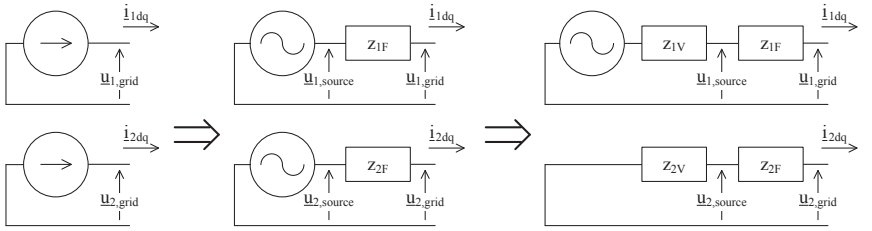


Figure 5.5: CBDG model used in the case studies

shows the equivalent current source model, the current controlled voltage source model and the equivalent model that is used here. z_{1F} and z_{2F} are the filter impedances. z_{1V} and z_{2V} are virtual impedances. The virtual impedances have a minimal value ($z_{1/2V,min}$) to obtain the equivalent gain of the voltage support:

$$k_1 = \frac{1}{|z_{1F} + z_{1V,min}|} \qquad k_2 = \frac{1}{|z_{2F} + z_{2V,min}|} \tag{5.6}$$

Here, all values are expressed in p.u. values and the approximation is made that $z_{1/2F}$ is purely inductive, or at least that $z_{1/2F} + z_{1/2V,min}$ can be considered mainly inductive. The virtual impedances are changed to control the positive and negative sequence currents. Blocking the negative sequence currents is thus represented by an infinite $z_{2V,min}$ ($k_2 = 0$) and in case of voltage support according to (5.4), $z_{2V,min}$ equals $z_{1V,min}$ ($k_2 = k_1$).

The active power of the CBDG unit can be changed by changing the angle of the voltage source, but it is always lower than the prefault active power as more power is not available. During faults, the CBDG units can deliver 120% of their nominal current. When required, the virtual impedances are increased to satisfy this limit. In reality, the CBDG unit generates the positive sequence voltage between z_{1V} and z_{1F} and the negative sequence voltage between z_{2V} and z_{2F} to control the positive and negative sequence current. The current limitation is applied for the phase currents and is included in the iteration to obtain a limitation like (2.8), see section 2.4.3.

The total voltage that can be generated by the CBDG unit is of course limited. When SVM is assumed, this limit is[5]:

$$|\underline{u}_1| + |\underline{u}_2| \leq u_{\text{lim}} = 1.2 \text{ p.u.} \tag{5.7}$$

[5]The space vector will be an ellipse when both positive and negative sequence voltages are generated, see section 2.4.3, which is required to block the negative sequence current. This results in the limitation that the sum of the positive and negative sequence voltage has to be within the voltage limit of the converter to avoid overmodulation (5.7).

where, in this case study, the voltage limit is chosen to be 1.2 p.u., compared to the nominal voltage level. This is a 9% margin over the 1.1 p.u. maximum voltage that can be expected in normal operation. As discussed in section 5.2.1, the voltage is increased in the healthy phases when only positive sequence currents are injected into unbalanced faults [50,134]. When the voltage increases too much, this can lead to a disconnection of the CBDG units [135] or to overmodulation, see section 5.2.1. To avoid this, the voltage limit is imposed in the control scheme and in case of only positive sequence reactive current injection, the current is limited to fulfil (5.7), similar to the suggestions in publication [50] and in section 5.2.1.

The loads are modelled as constant impedances. More advanced load models (e.g. the ZIP model [147],[148]) exist, but they are usually only valid for (limited) balanced voltage dips. Traditional fault calculations often neglect loads completely, but the results will show that this is no longer allowed for certain scenarios.

Based on the calculations, the current and voltage phasors in the system are known in phase coordinates. These results are converted to symmetrical components for interpretation of the results. Additionally, the power transfer of the sources is calculated based on the approach given in [39, 59]. The relationship of the power transfer with the results in phase coordinates is detailed in appendix A.3.

Although the calculation method solves the three-phase network without using symmetrical components, studying the fault in symmetrical components is useful for interpretation of the results. The equivalent, simplified sequence scheme for the line-to-line fault at bus B (fault location F1) for scenarios 4-5 is given in Figure 5.6. In case of negative sequence current blocking (scenario 4), the negative sequence virtual impedances Z_{2V} of both sources are infinite. This means that the negative sequence current can only flow through the loads in the system. When there is at least one SG in the system, this SG provides a relatively low impedance path in the negative sequence. This already leads to the conclusion that the line-to-line fault current is determined by the loads when the negative sequence currents are blocked in scenarios with only power electronic sources. This is in line with the conclusions made in [67].

5.3.4 Results Line-to-Line Faults

In this section, faults F1 and F2 refer to line-to-line faults at location F1 and F2, see Figure 5.4. The fault currents (I_{sc} 2φ) for these faults are given in Table 5.2 for all scenarios. First, the only positive sequence voltage support, with negative sequence current blocking, and the positive and negative sequence

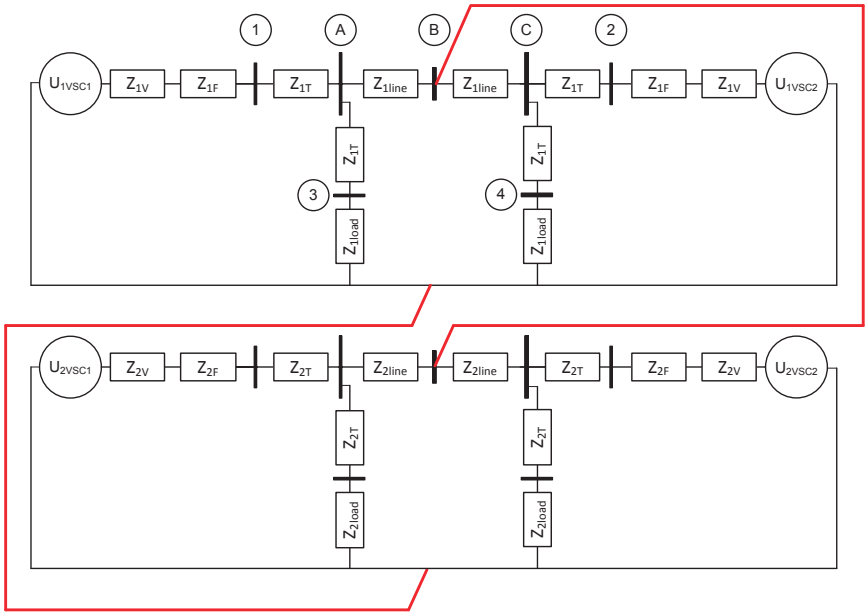


Figure 5.6: Small test system: sequence schemes for a line-to-line fault at bus B (Indices: V = virtual, F = filter, T = transformer)

Table 5.2: Fault currents for all scenarios of the small test system

No.	$\mathbf{I_{sc}}$ 2φ **F1** [kA]	$\mathbf{I_{sc}}$ 2φ **F2** [kA]	$\mathbf{I_{sc}}$ 1φ-e **F1** [kA]	$\mathbf{I_{sc}}$ 1φ-e **F2** [kA]	$\mathbf{I_{sc}}$ 2φ-e **F1** [kA]	$\mathbf{I_{sc}}$ 2φ-e **F2** [kA]
1	1.68	6.32	1.98	0.93	1.97-1.95	6.30-6.34
2	0.91	4.33	1.28	0.90	1.45-1.47	4.39-4.46
3	1.10	5.42	1.57	0.92	1.39-1.39	5.40-5.45
4	0.10	0.77	0.17	0.68	0.98-1.06	0.57-1.04
5	0.52	4.31	0.96	0.92	0.75-0.77	4.29-4.35
6	1.10	4.77	1.47	0.90	1.37-1.36	4.98-5.04

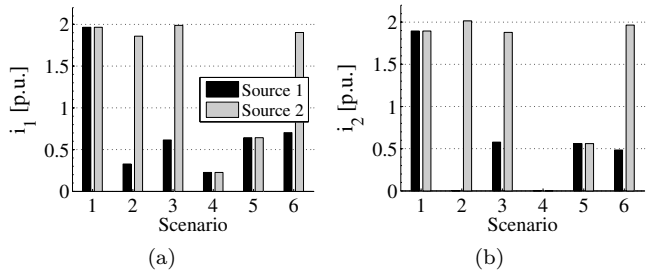


Figure 5.7: Line-to-line fault F1: (a) positive sequence current contribution i_1 and (b) negative sequence current contribution i_2 of source 1 and 2

voltage support strategies are compared. Scenario 6, with the current injection according to (5.5), is discussed at the end of this section.

It is immediately clear that negative sequence blocking by all sources results in much lower fault currents (scenario 4). As can be seen in Figure 5.6, the only path in the negative sequence is through the loads in this case. This results in fault currents of the order of magnitude of load currents. Increasing the fault current further is not allowed by the voltage limitation, as this would increase the positive sequence voltage and, together with the high negative sequence voltage, this would result in serious overvoltages. In case only one source blocks the negative sequence currents, the other source still delivers negative sequence currents and the fault currents are reduced much less (scenario 2). It is also clear that the limited current capacity of the VSCs compared to the SGs, mainly results in lower fault currents at the higher voltage level (fault F1). Due to the transformer impedance, the fault currents on the lower voltage level (fault F2) are reduced much less. In publication [49] and in chapter 4, section 4.3, similar conclusions were made for balanced faults.

The phasor results are converted to symmetrical components to allow an analysis of the results in both phasor and symmetrical components. Figure 5.7 shows the current contributions of both sources for the six scenarios. The negative sequence current blocking in scenario 2 and 4 is clearly visible from the results. The VSC sources also give a limited fault current, as their maximal current of 1.2 p.u. is divided between the positive and negative sequence current. The very low current contributions in scenario 4 are caused by the voltage limitation of the CBDG units. If SVM is assumed, the space vector of the CBDG units has to be within the limit (5.7) that can be generated.

The voltages for fault F1 are shown in Figure 5.8 and 5.9 in symmetrical components and in phase coordinates. Figure 5.8 shows how the voltages

change over the network. In case there is no negative sequence current injection on one side of the fault, the negative sequence voltage stays constant on that side. The higher current injections of the SGs result in more balanced voltages (higher positive sequence and lower negative sequence voltages) compared to the VSCs with negative sequence current injection, but the trends are similar. Figure 5.9 clearly shows the voltage increase in the healthy phase in case of negative sequence current blocking.

Finally, Figure 5.10 shows the amplitude of the maximal current on the left side of the fault and on the right side of the fault. Here, the difference between blocking and injecting negative sequence current is also clear. The figure also shows the oscillating power p_{var}. In appendix A.3, it is shown that the power oscillations, in absence of zero sequence components, can be calculated based on the phasor calculations with (A.5). The results of these calculations are presented here. In scenario 2, it is clear that the lack of negative sequence current injection by the VSC unit causes the SG to inject more negative sequence current and to have a higher oscillating power. In scenario 4, the units have a low oscillating power because they only inject a small current (see Figure 5.7) due to the voltage limitation (5.7). Consequently, they do not provide much voltage support (see Figure 5.8: the positive and negative sequence voltage at bus A and C are almost the same as the positive and negative sequence voltage at the fault location).

When fault F2 is analysed, similar results are found. Table 5.2 illustrates that blocking negative sequence currents results in a large reduction of the fault current if there is no other source that delivers negative sequence currents (scenario 4). However, this reduction is limited if there is still a SG in the system (scenario 2). The current contributions of the sources are given in Figure 5.11 and the voltages in the system are given in Figure 5.12 and 5.13. Fault F2 is behind bus A. This explains the shape of the curves, with a higher positive sequence and a lower negative sequence voltage at bus C, if source 2 delivers negative sequence current to the fault. This is the case for all scenarios except for scenario 4. Due to the wye-delta transformer between the fault and bus A/C, the line-to-line voltages now experience an overvoltage instead of the line-to-ground voltages, as was the case for fault F1. In Figure 5.14, the power oscillations show a similar trend as in Figure 5.10b: if only one source injects negative sequence current (scenario 2), it experiences a higher power oscillation. In scenario 4, the sources only inject a small current, resulting in little voltage support, but also in small power oscillations.

Scenario 6, with a negative sequence voltage support according to strategy (5.5), is included to illustrate that this approach leads to a voltage boost, but the effect is less pronounced compared to the negative sequence current blocking. The fault currents are also decreased, but again the effect is less pronounced.

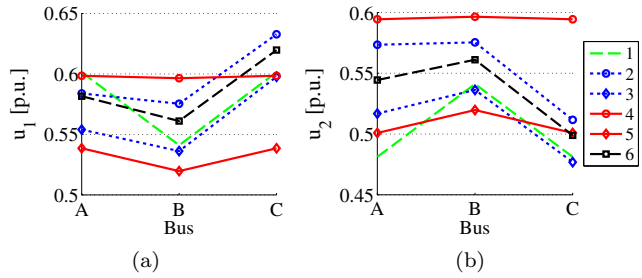


Figure 5.8: Line-to-line fault F1: (a) positive sequence voltage u_1 and (b) negative sequence voltage u_2 at bus A, B and C

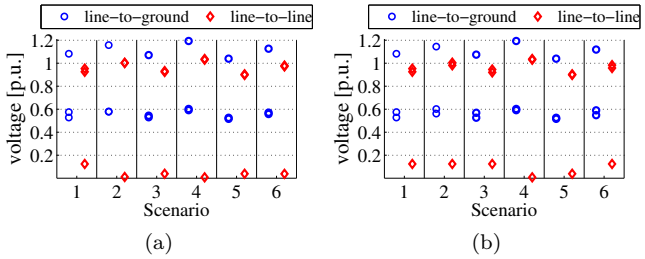


Figure 5.9: Line-to-line fault F1: (a) Voltages at bus A and (b) at bus C

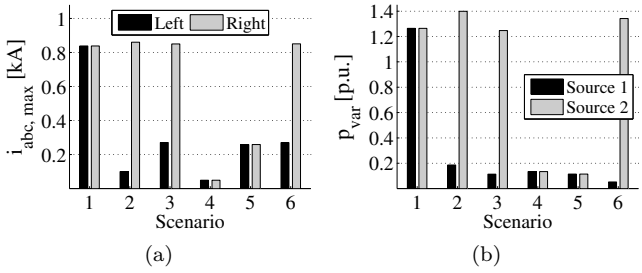


Figure 5.10: Line-to-line fault F1: (a) Maximum phase current on both sides of the fault and (b) the power oscillation of both sources

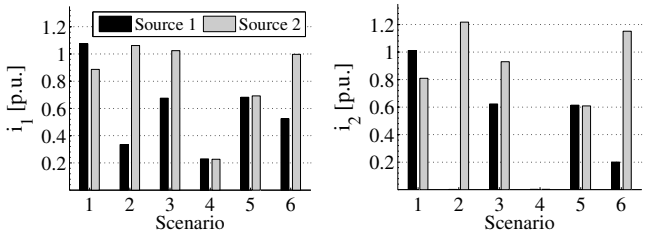


Figure 5.11: Line-to-line fault F2: (a) positive sequence current contribution i_1 and (b) negative sequence current contribution i_2 of source 1 and 2

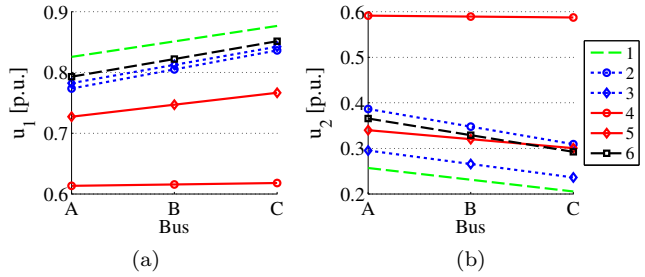


Figure 5.12: Line-to-line fault F2: (a) positive sequence voltage u_1 and (b) negative sequence voltage u_2 at bus A, B and C

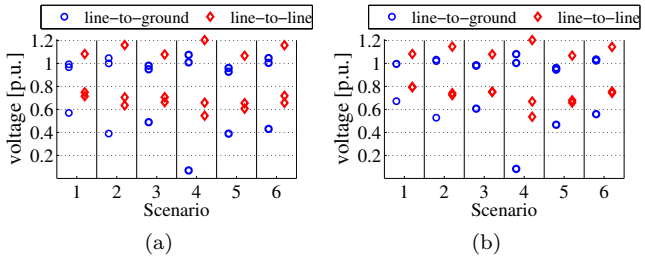


Figure 5.13: Line-to-line fault F2: (a) Voltages at bus A and (b) at bus C

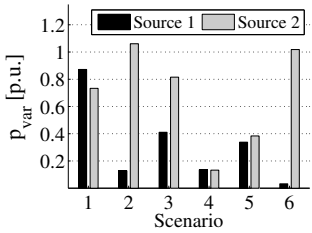


Figure 5.14: Line-to-line fault F2: the power oscillation of both sources

From Figure 5.10b and 5.14, it is also clear that the power oscillation of the SG (= Source 2) is increased because the VSC unit does not take its full share of negative sequence current (scenario 6 $\leftrightarrow$ scenario 3). For a fault electrically closer to the VSC unit (F1), this voltage support strategy is closer to strategy (5.4) than for a fault further away (F2)[6].

For a scenario with only VSC units in the system, strategy (5.5) can only be realised by limiting the currents significantly. Otherwise, the voltage rise is too big. Alternatively, a current in between strategies (5.4)-(5.5) can be used. These intermediate strategies are not reported, but they have been evaluated and the results are always in between scenario 4 and 5.

5.3.5 Results Single-Line-to-Ground Faults

In this section, faults F1 and F2 refer to single-line-to-ground faults at location F1 and F2, see Figure 5.4. The fault currents (I_{sc} 1φ-e) for these faults are given in Table 5.2 for all scenarios. The figures of the detailed analyses of the results are listed in appendix C.1.1.

The results show a similar trend as for the line-to-line faults. Of course, for a single-line-to-ground fault, the zero sequence scheme plays an important role. However, when the negative sequence current is blocked, lower fault currents are noticed. Even when the fault current is mainly determined by the earthing transformer, i.e. for fault F2, the reduction in scenario 4 is obvious. In scenario 6, the current of source VSC1 has to be limited to fulfil the voltage limit (5.7) and obtain currents according to strategy (5.5).

The other conclusions concerning the voltage rise and the power oscillations, are also valid for the single-line-to-ground faults. The zero sequence voltage

[6]Close to line-to-line faults, positive and negative sequence voltage are both roughly 0.5 p.u. ($u_1 \simeq u_2 \approx 0.5$ p.u.) and both approaches give similar results, but further away from the fault, the approaches are different.

on the 110 kV level is also shown in appendix C.1.1. For fault F2, there is no zero sequence voltage at the 110 kV level, as the DT blocks the zero sequence currents and voltages.

5.3.6 Results Two-Lines-to-Ground Faults

In this section, faults F1 and F2 refer to two-lines-to-ground faults at location F1 and F2, see Figure 5.4. The fault currents (I_{sc} 2φ-e) for these faults are given in Table 5.2 for all scenarios. The results show two fault currents, as the currents in both faulted phases are different. The figures of the detailed analyses of the results are listed in appendix C.1.2.

Of course, for a two-lines-to-ground fault, the zero sequence scheme plays an important role. For fault F2, a similar trend is noticed as for the line-to-line and the single-line-to-ground fault. For scenario 6, the current of source VSC1 has to be limited, similar to scenario 6 for the single-line-to-ground fault at location F2.

For fault F1, the limited short-circuit power of the system, and the coupling of the positive, negative and zero sequence schemes at the location of the fault, causes lower zero sequence voltages in scenario 5 (no negative sequence current blocking) than in scenario 4 (negative sequence current blocking). This causes smaller zero sequence currents through the earthing of the DT and smaller line-to-ground voltages. This mainly illustrates the importance of a high short-circuit power, as already stated in chapter 4. For the remainder of this discussion, the conclusions concerning the power oscillations remain valid for fault F1, but overvoltages never occur.

5.3.7 Interpretation of the Results

As is clear from the results, blocking the negative sequence current during unbalanced faults leads to very low fault currents if there are no other sources in the system that provide negative sequence currents. If there are other sources that provide negative sequence currents, the effect of a unit that blocks the negative sequence current is more limited. Especially on the lower voltage levels, the fault currents are not reduced drastically in that case. These lower voltage levels are more likely to have simple overcurrent relays. Therefore, a strong reduction of the fault currents on the lower voltage levels would require a complete redesign of the protection system.

When some CBDG units inject only positive sequence current during unbalanced faults, the stress on the other generation units (e.g. SGs or CBDG units in

the system that apply the positive and negative sequence voltage support) is increased, as they experience a higher power oscillation. The reason for this higher power oscillation is that the positive sequence voltage is boosted, but the negative sequence voltage is not reduced by this only positive sequence current injection. Therefore, the other generation units will inject a relatively higher negative sequence current and a relatively smaller positive sequence current. However, these injections result in higher power oscillations for these other generation units.

Additionally, the voltage in the healthy phase is boosted when some CBDG units inject only positive sequence current during unbalanced faults. In a heterogeneous system, where several CBDG units have different voltage limitations, it is possible that some units boost the voltage above the limit of the other units and that these other units have to disconnect from the system.

Therefore, based on this limited system, applying the positive and negative sequence voltage support strategy (5.4), and thus injecting negative sequence currents into the system during unbalanced faults, seems beneficial for three reasons. This avoids the very low fault currents, the higher power oscillations of the other generation units and the overvoltages in the system.

From a system perspective, and especially in case of a high share of CBDG, the positive and negative sequence voltage support strategy (5.4) is better than the alternative strategy (5.5), as the overall voltage unbalance in the system is decreased, the voltage in the healthy phase is not boosted and there is no additional stress on the remaining SGs. From a CBDG perspective, strategy (5.5) leads to lower power oscillations and it is certainly better than negative sequence current blocking. So for lower CBDG shares in the grid, it could be considered as a valid option. However, as described already in section 5.2.3, it is not a suitable strategy for the grid. The post-fault behaviour of this strategy is not clearly defined and this issue should be tackled before using this strategy. If the amount of CBDG units is very limited, not participating in the fault currents can also be an option. The CBDG units then simply stay standby (FRT without voltage support for unbalanced faults).

As a final remark, it should be noted that the current limitation of the converter of the CBDG unit plays a role during faults near the CBDG unit. When negative sequence reactive current is injected, the positive sequence current, and also the active current, has to be reduced. A study focussing on these trade-offs, described in publication [114], shows that negative sequence current injection during unbalanced faults limits the active power transfer capability. Especially for HVDC transmission, this can be a drawback in certain scenarios [114]. In the case study described here, the active power demand from the loads during the unbalanced fault also decreases and therefore, the active power reduction of

the CBDG units is no issue.

5.4 Effect of Blocking versus Injecting Negative Sequence Current - Case Study in a Larger Test System

In this section, a larger test system is analysed during unbalanced faults with different current injection strategies. Two strategies are investigated: (1) only positive sequence voltage support with negative sequence current blocking and (2) the positive and negative sequence voltage support according to (5.4). In literature, these strategies are only evaluated in grids with a limited amount of CBDG units or with locally concentrated CBDG units. The ILNEM calculation framework, developed in chapter 3, allows to evaluate these strategies in grids with a high share of CBDG.

First, the test system and the scenarios are introduced. The calculation method is the same as the one explained in section 5.3.3. The active power transfer of all sources is kept lower than the prefault active power transfer. Afterwards, line-to-line and single-line-to-ground faults are analysed and finally, the results are interpreted.

5.4.1 System Description

The same nine bus system that was used in section 4.3, is used in this case study. This system is inspired on the WECC nine bus system with three SGs (SG1-SG3) [113], but the line lengths are modified and there are no loads on the 230 kV voltage level. It is extended with three subgrids that are identical with respect to their transformer and line parameters, see Figure 5.15. All loads and CBDG units are connected to the 15 kV MV level of the subgrids and they are distributed equally over the DTs. Both the PTs and the DTs in the subgrid have tap changers on the primary side to control the voltages at their secondary side. The generator, transformer and line data are given in appendix B: Table B.1, B.2 and B.3. The CBDG and load data for this case study are given in Table 5.3.

As is clear from the results of the small test system in section 5.3, the blocking of the negative sequence currents has the largest influence when there are no or only a few SGs in the system. Therefore, two configurations of the system are investigated. In the first configuration, SG2 and SG3 are out of service and

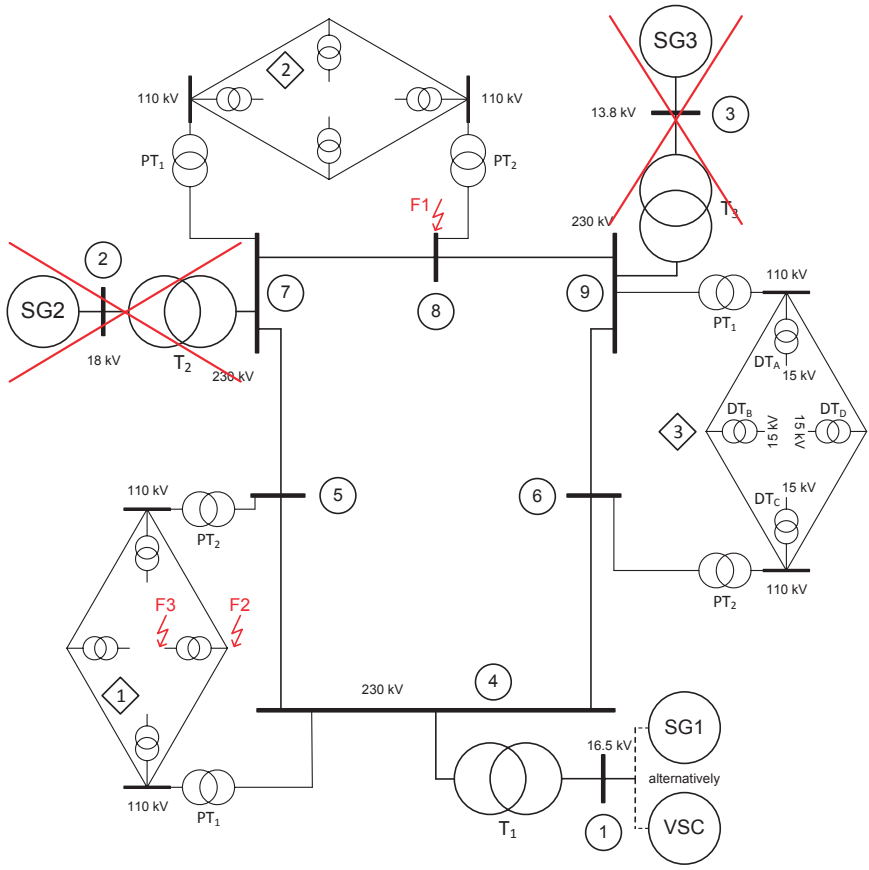


Figure 5.15: Test system: extension of WECC nine bus system (Fault locations are indicated with a lightning symbol and crosses indicate elements that are out of service.)

Table 5.3: Load and CBDG data for the test system (all values are given in the load sign convention)

Subgrid	**1**	**2**	**3**
P_{load} [MW]	125	90	100
Q_{load} [MVAr]	31.25	22.5	25
P_{CBDG} [MW]	-82.07	-68.75	-75.69
Q_{CBDG} [MVAr]	-18.09	-10.19	-12.01
$S_{CBDG,nom}$ [MVA]	192	192	192

Table 5.4: Detailed data of the PTs with vector group Yyd
(notation according to [24], H = primary, M = secondary, L = tertiary)

$\mathbf{S_{nom}}$	$\mathbf{U_{prim}}$	$\mathbf{U_{sec}}$	$\mathbf{z_{1HM}}$	$\mathbf{z_{0HL}}$	$\mathbf{z_{0ML}}$	$\mathbf{z'_{0H}}$
200 MVA	230 kV	110 kV	20 %	20 %	20 %	15 %

the CBDG units in the subgrids feed all the loads together with SG1. In the second configuration, SG1 is also out of service, but it is replaced by a converter interfaced source, VSC, e.g. representing a HVDC connection or a WPP. In this configuration, all units in the system can block the negative sequence current.

For faults including ground, the earthing system is important, as it has a large influence on the zero sequence impedances. In this case study, the starpoints of transformers T_1, T_2 and T_3 are isolated. The PTs have a tertiary delta compensation winding. The starpoint of the primary side (230 kV level) is earthed directly and the starpoint of the secondary side (110 kV level) is earthed over a reactor with an impedance of 2.02 Ω. The detailed data of the PTs, with notation according to [24], is given in Table 5.4. In the positive and negative sequence scheme, this transformer is equivalent to the PT specified in Table B.2. The starpoints of the primary side of the DTs are isolated. On the secondary side of all DTs, an earthing transformer, that gives a theoretic single-line-to-ground fault of 1000 A, is connected. For the zero sequence impedances of the 230 kV lines, no information is available in [113]. Based on examples in the IEC 60909 standard [86], the assumption is made that $R_0 = 3.5 \cdot R_1$ and $X_0 = 3.5 \cdot X_1$, see Table B.3.

5.4.2 Scenarios

The different scenarios are listed in Table 5.5. Source 1 is either SG1 or VSC. The negative sequence currents are either blocked or the positive and negative sequence voltage support strategy (5.4) is applied. The gain k of the voltage support (5.4) can be related to the sum of the virtual and fixed impedance used in the calculations with (5.6), as described in section 5.3.3. Note that the gain of the voltage support is given at the terminals of the CBDG unit. Including the transformer impedance, the gain is significantly lower. Nevertheless, one scenario (VSC-n-low-k) is repeated with a lower gain. One scenario is also repeated with a lower load (VSC-p-load2).

Three fault locations at different voltage levels are considered (F1, F2 and F3 in Figure 5.15). First, line-to-line faults are discussed. Afterwards, single-line-to-ground faults are investigated. Although these single-line-to-ground

Table 5.5: Scenarios for the test system

Scenario	**Source 1**	$\mathbf{k_1}$	$\mathbf{k_2}$	$\mathbf{S_{CBDG,tot}}$	$\mathbf{k_1}$	$\mathbf{k_2}$
SG-n	SG1	/	/	576 MVA	4	4
SG-p	SG1	/	/	576 MVA	4	0
VSC-n	VSC	5	5	576 MVA	4	4
VSC-np	VSC	5	5	576 MVA	4	0
VSC-p	VSC	5	0	576 MVA	4	0
VSC-n-low-k	VSC	2.86	2.86	576 MVA	2	2
VSC-p-load2	VSC	5	0	576 MVA	4	0

Legend: SG: Source 1 = SG1; VSC: Source 1 = VSC; n: The CBDG units (including VSC) provide positive and negative sequence voltage support; p: The CBDG units (including VSC) only provide positive sequence voltage support; np: Source 1 (= VSC) = n, CBDG units = p; low-k: lower gain of voltage support; load2: lower load in the grid (half of other scenarios)

faults are highly dependent on the zero sequence impedances (i.e. the earthing system of the network), they also depend on the negative sequence behaviour of the system. Therefore, the effect of the negative sequence current blocking or injection is also investigated for single-line-to-ground faults.

5.4.3 Results Line-to-Line Faults

In this section, F1, F2 and F3 refer to line-to-line faults at fault locations F1, F2 and F3 respectively, see Figure 5.15. Table 5.6 and 5.7 show a selection of the results for all scenarios.

Table 5.6 lists the total fault current (I_{sc}) for each of the three faults. The table also gives the oscillating power p_{var}, as defined in appendix A.3 (A.5), and the positive and negative sequence reactive current for source 1 (i.e. SG1 or VSC), expressed in the generator sign convention. This positive sequence reactive current is the total reactive current, (the load flow has a I_{1q} of $-0.39\,kA$). It can be seen from the results that when the CBDG units don't provide negative sequence currents, the fault current reduces (SG-p $\leftrightarrow$ SG-n: $-30\% \rightarrow -18\%$ and VSC-n $\leftrightarrow$ VSC-np: $-45\% \rightarrow -19\%$). In addition, source 1 delivers more negative sequence current and therefore, source 1 experiences a larger oscillating power (SG-p $\leftrightarrow$ SG-n: $+32\% \rightarrow +128\%$ and VSC-n $\leftrightarrow$ VSC-np: $+57\%$

Table 5.6: Results for the line-to-line faults on the test system (1)

Scenario	**Fault**	$\mathbf{I_{sc}}$ [kA]	**Source 1** $\mathbf{p_{var}}$ [p.u.]	$\mathbf{I_{1q}}$ [kA]	$\mathbf{I_{2q}}$ [kA]
SG-n	F1	2.7	0.81	-11.0	10.0
SG-n	F2	4.0	0.59	-7.0	6.2
SG-n	F3	10.2	0.18	-2.1	1.6
SG-p	F1	1.9	1.07	-10.2	12.8
SG-p	F2	2.9	0.90	-7.0	9.4
SG-p	F3	8.4	0.41	-1.9	3.6
VSC-n	F1	2.0	0.23	-5.3	4.8
VSC-n	F2	3.7	0.41	-5.4	4.9
VSC-n	F3	10.2	0.16	-1.9	1.5
VSC-np	F1	1.1	0.36	-4.1	5.9
VSC-np	F2	2.3	0.46	-4.2	6.1
VSC-np	F3	8.3	0.38	-1.7	3.4
VSC-p	F1	0.7	0.15	-0.6	0.0
VSC-p	F2	1.5	0.14	-0.7	0.0
VSC-p	F3	7.3	0.08	-0.8	0.0
VSC-n-low-k	F1	2.0	0.23	-5.2	4.9
VSC-n-low-k	F2	3.4	0.35	-5.1	4.6
VSC-n-low-k	F3	9.6	0.15	-1.9	1.5
VSC-p-load2	F1	0.4	0.22	0.7	0.0
VSC-p-load2	F2	0.8	0.21	0.4	0.0
VSC-p-load2	F3	5.0	0.13	0.1	0.0

Table 5.7: Results for the line-to-line faults on the test system (2)

Scenario	**Fault**	**DG sub 1A** $\mathbf{p_{var}}$ [p.u.]	**DG sub 1B** $\mathbf{p_{var}}$ [p.u.]	**DG sub 2B** $\mathbf{p_{var}}$ [p.u.]
SG-n	F1	0.30	0.31	0.20
SG-n	F2	0.24	0.12	0.29
SG-n	F3	0.21	0.10	0.09
SG-p	F1	0.24	0.23	0.23
SG-p	F2	0.21	0.25	0.15
SG-p	F3	0.09	0.29	0.05
VSC-n	F1	0.25	0.26	0.19
VSC-n	F2	0.22	0.12	0.31
VSC-n	F3	0.21	0.10	0.09
VSC-np	F1	0.24	0.24	0.24
VSC-np	F2	0.23	0.26	0.17
VSC-np	F3	0.10	0.29	0.05
VSC-p	F1	0.32	0.32	0.24
VSC-p	F2	0.37	0.41	0.22
VSC-p	F3	0.19	0.46	0.13
VSC-n-low-k	F1	0.25	0.25	0.19
VSC-n-low-k	F2	0.21	0.14	0.21
VSC-n-low-k	F3	0.15	0.14	0.09
VSC-p-load2	F1	0.10	0.11	0.12
VSC-p-load2	F2	0.11	0.12	0.11
VSC-p-load2	F3	0.10	0.23	0.09

$\rightarrow +138\%$), even for faults at lower voltage levels. Thus, the blocking of the negative sequence currents increases the stress on the units that provide negative sequence currents. When all units block the negative sequence currents (VSC-p), the fault current is determined by the loads in the system. It is much lower, especially at the higher voltage levels (VSC-p $\leftrightarrow$ VSC-n: -65% on 230 kV (F1) $\rightarrow -28\%$ on 15 kV (F3)). To illustrate the dependence on the load, the simulation is repeated with a low load scenario, where all loads are reduced by a factor of two. As can be seen from the results (VSC-p-load2 $\leftrightarrow$ VSC-p), the fault currents are reduced significantly. In addition, the negative sequence voltages in these scenarios are high throughout the system, even for fault F3, located on the 15 kV voltage level (u_2 on 230 kV voltage level: 0.49 p.u. for VSC-p-load2 and 0.35 p.u. for VSC-p). To avoid overmodulation, the positive sequence voltage is also reduced (e.g. u_1 on 230 kV voltage level: 0.69-0.70 p.u. for VSC-p-load2 and 0.82-0.83 p.u. for VSC-p). In the low load scenario, the reactive current injection of the VSC source even changes sign to avoid (too high) overvoltages. As a consequence, a fault on a lower voltage level has an impact throughout the entire network. Therefore, in this case, blocking the negative sequence currents is a bad strategy, as the reliability of the grid reduces significantly.

Table 5.7 shows the oscillating power for three CBDG units in the system: in subgrid 1 unit A and B (F2 and F3 are close to unit B) and in subgrid 2 unit B (this unit is further away from fault F2 and F3, but closest to fault F1). This table is included to illustrate the effect of negative sequence current contributions on the CBDG units. As explained in section 5.2.3, several papers have mentioned that injecting negative sequence into an unbalanced fault according to the ratio of the voltages (strategy (5.5)), reduces the power oscillations [135, 140]. The closer to the line-to-line fault, the more this strategy is in line with strategy (5.4) that is used here: injection according to the change in positive and negative sequence voltage. Therefore, sometimes the CBDG unit closest to the fault has a lower oscillating power than a unit further away from the fault. In case of negative sequence blocking, the oscillating power is sometimes lower because the units only inject a small current. However, as mentioned earlier, there is then almost no voltage support. Scenario VSC-n-low-k illustrates that reducing the gain of the voltage support can reduce the oscillating power a little bit for faults further away, but the fault currents are also reduced a bit.

5.4.4 Results Single-Line-to-Ground Faults

In this section, F1, F2 and F3 refer to single-line-to-ground faults at fault locations F1, F2 and F3 respectively, see Figure 5.15. Table C.1 and C.2 in appendix C.2.1 show a selection of the results for all scenarios.

The results show a similar trend as in the previous section. Blocking the negative sequence current decreases the fault currents, except for fault F3, where the earthing transformer has a large zero sequence impedance and the negative sequence impedance of the loads is sufficiently small to have no real reduction of the single-line-to-ground fault currents. For the other faults, the reduction is clear (e.g. VSC-p $\leftrightarrow$ VSC-n: -62% on 230 kV (F1) $\rightarrow$ -53% on 110 kV(F2)). Furthermore, when the CBDG units block the negative sequence currents, the stress on the remaining SG increases due to the higher power oscillations (SG-p $\leftrightarrow$ SG-n: $+44\%$ $\rightarrow$ $+77\%$ for faults F1 and F2). The dependence of the fault currents on the loads in scenarios where the negative sequence current is blocked by all sources, is clear by comparing VSC-p and VSC-p-load2: the fault currents at 230 kV (F1) and 110 kV (F2) are strongly dependent on the loads in these scenarios.

The analysis of the single-line-to-ground faults thus leads to similar conclusions as the analysis of the line-to-line faults. As the single-line-to-ground faults at the 15 kV level are mainly determined by the earthing transformer, the faults at this level have no high impact on the higher voltage levels. In case of a different earthing system, higher single-line-to-ground fault currents are possible. In that case, blocking the negative sequence currents will also lead to a higher impact of these faults on the higher voltage levels, similar to the line-to-line faults.

5.4.5 Interpretation of the Results

From the results[7], it is clear that the fault currents are reduced when the CBDG units block the negative sequence currents. When there is still a SG in the system, the reduction is more limited. In the scenario without sources that inject negative sequence currents, the fault currents in the system depend on the load model. This was illustrated by changing the loads and noticing a significant change in fault currents. It should be noted that accurate load models during (unbalanced) faults are not available in literature.

When the positive and negative sequence voltage support is applied, the fault currents are reduced much less, especially on the lower voltage levels. As mentioned already in section 5.3.7 and in chapter 4, section 4.3.4, a reduction of the fault currents on the lower voltage levels can have a large impact on the protection systems at these voltage levels, as these protection systems rely

[7]This interpretation is mainly based on the interpretation of the line-to-line faults. Most of these interpretations are also valid for the single-line-to-ground faults, or at least for some earthing systems, i.e. the earthing systems that result in large single-line-to-ground fault currents. Nevertheless, when only one fault type gives good arguments to choose a certain fault current contribution strategy, and there are no drawbacks for the other fault types, this strategy should be chosen as no fault type can be excluded totally.

on the magnitude of the fault currents. Especially for European MV and LV grids, the impact of CBDG units on the protection system is limited if the fault currents, supplied by the higher voltage levels to the fault, are not reduced (significantly). Changes to the protection systems at these voltage levels are then only required when the CBDG units influence the local protection system, but this is usually not the case or the problems can be solved with local adaptations to the protection system. This means that applying the positive and negative sequence voltage support in scenarios with a high share of CBDG and little conventional generation avoids a complete redesign of the existing protection systems of typical European MV and LV grids.

As in the case study on the small test system in section 5.3, the remaining SG also experiences larger power oscillations, and thus more stress, when the negative sequence currents are blocked, compared to when the positive and negative sequence voltage support is applied. The voltage in the healthy phase is also boosted in case of negative sequence current blocking. In this case study, all CBDG units have the same voltage limit. However, in a heterogeneous system, where several CBDG units have different voltage limitations, it is possible that some units boost the voltage above the limit of the other units. These other units then have to disconnect from the system. When the positive and negative sequence voltage support is applied, the voltage in the healthy phase is not boosted and the voltage system is more balanced during unbalanced faults.

In addition, the case study on a larger test system shows that when there are only a few SGs in the system or no SGs at all, and the CBDG units block the negative sequence currents, the negative sequence voltages in the system are not reduced (significantly). Due to the voltage limitation of the CBDG units, this also implies that the positive sequence voltage in the system is lower. As a consequence, faults at lower voltage levels start having a larger impact on higher voltage levels. This should be avoided at all cost, as the reliability of the grid then reduces significantly, i.e. the system is then disturbed for all faults at lower voltage levels. When the positive and negative sequence voltage support is applied, the impact of a fault at a lower voltage level on the higher voltage levels is limited. In that case, the negative sequence part of the fault currents, supplied from the higher voltage levels, through the transformers and other network elements, to the fault location at the lower voltage level, results in a much lower negative sequence voltage at the higher voltage levels than at the fault location. Likewise, the positive sequence voltage at the higher voltage level is then much higher than the positive sequence voltage at the fault location due to the positive sequence part of the fault currents.

5.5 Conclusion

Many different current injection strategies for CBDG units during unbalanced faults are suggested in literature. After a short review of these strategies, and based on the research performed in publication [50], three strategies are selected: (1) the only positive sequence voltage support with negative sequence current blocking and limitation to avoid overvoltages, (2) the positive and negative sequence voltage support and (3) an alternative positive and negative sequence reactive current injection strategy that focuses on limiting the power oscillations of the CBDG units. In literature, these strategies are only evaluated in grids with a limited amount of CBDG units or with locally concentrated CBDG units.

Also in this chapter, first a case study on a small test system, including the three strategies, is investigated. This case study shows that the third strategy obtains results in between the other two strategies, but increases the power oscillations of the remaining SGs compared to the positive and negative sequence voltage support strategy. In addition, this strategy defines reactive current injections and not additional reactive current injections like the other two strategies. It is unclear how this strategy will affect the system after fault clearing. Therefore, it is not considered as a suitable strategy.

The ILNEM calculation framework, developed in chapter 3, allows to study the strategies in scenarios where many CBDG units replace SGs, as was set forth in the objectives of this dissertation. Therefore, the two remaining strategies, i.e. (1) the only positive sequence voltage support with negative sequence current blocking and limitation to avoid overvoltages and (2) the positive and negative sequence voltage support, are studied on a larger test system. Based on the theoretical considerations, the case study on the small test system and a case study on the larger test system, the positive and negative sequence voltage support strategy has many advantages over an only positive sequence voltage support strategy, with negative sequence current blocking, during unbalanced faults.

If there is a significant number of SGs, blocking of the negative sequence currents by CBDG units during unbalanced faults has a relatively limited effect on the fault currents in the system. The remaining SGs experience a higher stress during the fault due to higher power oscillations. When the amount of SGs in the system decreases, the fault currents are also reduced. In case there are no SGs in the system, the fault currents become dependent on the loads and are very low. On the lower voltage levels, the reduction of the fault currents can also directly influence the operation of the protection systems, that rely on the magnitude of the fault currents. This would require a complete redesign of the existing protection systems of typical European MV and LV grids. Due to the

very low fault currents, a voltage dip at a lower voltage level is also experienced at higher voltage levels. Line-to-line faults, and in some cases other unbalanced faults, then have a significant impact on the higher voltage levels. This results in a reduced reliability of the grid. In addition, blocking the negative sequence currents and injecting positive sequence currents boosts the voltage. This can result in a disconnection of other CBDG units.

When the positive and negative sequence voltage support is applied, and thus positive and negative sequence reactive currents are injected, the remaining SGs do not experience additional stress. The reduction of the fault currents is limited, especially on the lower voltage levels. This avoids a complete redesign of the existing protection systems of typical European MV and LV grids. Changes to the protection systems at these voltage levels are then only required when the CBDG units influence the local protection system, but this is usually not the case or the problems can be solved with local adaptations to the protection system. There are no additional reliability concerns when this strategy is applied, as the fault currents are not reduced (significantly) and the impact of an unbalanced fault at a lower voltage level on the higher voltage levels is limited. Unlike with the negative sequence current blocking, there are no additional voltage rises, compared to the situation without CBDG units, during unbalanced faults.

Chapter 6

Conclusions

This chapter:

- summarises the main conclusions of this dissertation in section 6.1
- gives an overview of the chapters and the main contributions of this work in section 6.2
- lists recommendations to the different stakeholders in section 6.3
- gives an outlook on possible future research in section 6.4

6.1 General Conclusions

In the future, there will be more and more Distributed Generation (DG) units in the grid and more of these DG units will be Converter Based Distributed Generation (CBDG) units. The fault behaviour of these CBDG units is a design parameter as their control systems are able to control the fault current contributions. The effect of the current contribution of CBDG units, during both balanced and unbalanced faults, can be positive or negative for the grid. To evaluate these effects in scenarios with a high share of CBDG, a simplified calculation framework is developed and validated in this dissertation. It is shown that CBDG units, with the appropriate voltage support settings, can contribute to the short-circuit power of the grid. When CBDG units provide only positive sequence voltage support during unbalanced faults, and thus block negative sequence currents, this can lead to very low fault currents in scenarios

with a high share of CBDG and little conventional generation. These low fault currents would require a complete redesign, including huge investment costs, of all existing protection systems at the lower voltage levels of the grid, as these protection systems rely on the magnitude of the fault currents. In addition, very low fault currents result in a reduced reliability of the grid, as faults at lower voltage levels then have a significant impact on the higher voltage levels. The remaining Synchronous Generators (SGs) in the grid also experience additional stress when CBDG units only provide positive sequence voltage support during unbalanced faults. When CBDG units provide both positive and negative sequence voltage support, these drawbacks are avoided.

In summary, with the appropriate voltage support settings for CBDG units, the balanced and unbalanced fault currents are not reduced significantly, especially at the lower voltage levels, in scenarios with a high share of CBDG and little conventional generation. For the faults at the lower voltage levels, a high fault current flows from the higher voltage levels to the fault at the lower voltage level. This high fault current is delivered by many different CBDG units in the grid. When the fault currents remain high on the lower voltage levels, the existing protection systems at these voltage levels do not require a complete redesign and faults on these voltage levels do not have a significant impact on the higher voltage levels. This way, the CBDG units adequately replace the conventional generation from a fault behaviour point of view.

6.2 Chapter Overview and Main Contributions

In *chapter 1*, the context of this dissertation is situated and the main research objectives are introduced. They are all related to the main research question, i.e. what is the influence of many CBDG units, that replace SGs in the network, on the fault currents and voltages in the network during balanced and unbalanced faults. The objectives of the dissertation are to:

- Demonstrate that the fault behaviour of CBDG units is a design parameter.
- Investigate and develop simplified methods to study fault currents and fault voltages in scenarios with a high share of CBDG.
- Investigate the influence of the voltage support settings of CBDG units on the short-circuit power of the grid.
- Evaluate different fault current contribution strategies for CBDG units during unbalanced faults in scenarios with a high share of CBDG.

The demonstration that **the fault response of CBDG units is a design parameter**, is described in *chapter 2*. Examples of control systems for CBDG units and their flexible fault response are given. The positive and negative sequence current injection of a CBDG unit can be controlled separately. Whenever negative sequence currents are injected, the current limitation of the CBDG units has to take into account both the positive and negative sequence currents. An optimal current limitation can, depending on the angles of both the positive and negative sequence current phasors, provide 0-15 % more current compared to a simple addition of the positive and negative sequence currents. During low negative sequence voltages, it is a challenge to inject negative sequence currents with a defined angle and therefore, a deadband for this injection is often applied. After fault clearing, the negative sequence current injection should be reduced promptly to avoid a negative influence on the voltage recovery after the fault.

To evaluate scenarios with a high share of CBDG, and a reducing share of conventional SGs, simulation models that accurately model the fault behaviour of CBDG units are required. These are discussed extensively in *chapter 3*. EMT simulation with switched models are considered too computationally intensive to model scenarios with multiple CBDG units. Averaged Value Models (AVMs) can be used instead of switched models. These AVMs are more than 15 times faster and are capable of accurately modelling the (fault) behaviour of CBDG units up to one-third to half of the switching frequency of the power electronic converters. Therefore, they can be used as reference models for fault studies. In this chapter, **the Iterative Linear Network Equations Method (ILNEM) is suggested as the simplest method that is capable of taking into account the control behaviour of CBDG units during faults**. Similar methods were suggested in literature, but they were not demonstrated in grids with multiple CBDG units. In this case, convergence issues can occur. After a **fine-tuning of this method**, with additional iterations and smaller step sizes, a smooth convergence to realistic solutions is assured. This method is validated with EMT simulations, that use AVMs, to demonstrate the accuracy of the method. The main limitations to this method are the limited accuracy of the SG model, that does not take into account saliency, and the fact that the motion equations and the frequency behaviour are not taken into account. These effects are however limited for short fault durations.

Balanced faults are investigated in *chapter 4*. In literature, much research on transient stability, Fault Ride Through (FRT) requirements, the optimal phase angle of the current injections for voltage support, ... is performed already, but there are still doubts about the effect of many CBDG units replacing SGs. Sometimes, even unrealistic assumptions on the short-circuit power evolution are made in literature. In this work, it is shown that **CBDG units can**

contribute to the short-circuit power in the grid, also at the higher voltage levels, depending on the voltage support settings. This way, the CBDG units limit the drop in short-circuit power at the higher voltage levels when they replace conventional generation. When this reduction of the short-circuit power at the higher voltage levels is limited, the fault currents at the lower voltage levels, supplied by the higher voltage levels, do not change significantly. The protection systems of typical European MV and LV grids rely on the magnitude of these fault currents. Therefore, **applying the appropriate voltage support settings in scenarios with a high share of CBDG and little conventional generation avoids a complete redesign of the existing protection systems of all typical European MV and LV grids**. Locally, the voltage support of CBDG units can result in a (limited) increase of the short-circuit power. The voltage support can then be applied until the short-circuit power limits of the local grid are reached.

Different current contribution strategies for CBDG units during unbalanced faults are evaluated in *chapter 5*. When only positive sequence voltage support is given during unbalanced faults, and thus negative sequence currents are blocked, this can lead to a considerable voltage increase in the healthy phases. The voltage increase can be reduced by limiting the positive sequence voltage support or by applying a positive and negative sequence voltage support, where an additional capacitive positive sequence current and an inductive negative sequence current are injected. These effects are described in literature, but are only evaluated in grids with a limited amount of CBDG units. In this dissertation, **the calculation framework from chapter 3 is used to evaluate these strategies in scenarios with a high share of CBDG**. This confirms the results from literature and leads to new insights in the effects of applying these different strategies in these scenarios. **When CBDG units block the negative sequence currents and use the limited version of the positive sequence voltage support, the fault currents during unbalanced faults are reduced**. When there are no remaining SGs in the system, the fault currents are of the order of magnitude of the load currents and they depend on the loads in the system. On the lower voltage levels, the reduction of the fault currents directly influences the operation of the protection systems, that rely on the magnitude of the fault currents. This would require a complete redesign of the existing protection systems of all typical European MV and LV grids. In addition, very low fault currents result in a reduced reliability of the grid, as faults at lower voltage levels then have a significant impact on the higher voltage levels. Remaining SGs (or CBDG units that provide negative sequence voltage support) also experience higher stress during the fault, i.e. a higher oscillating power transfer, when some CBDG units only provide positive sequence voltage support during unbalanced faults. **When positive and negative sequence voltage support is applied, the fault currents**

are reduced much less, especially at the lower voltage levels. The fault currents at these lower voltage levels are then mainly supplied by the higher voltage levels, similar to the situation without CBDG units. **This avoids a complete redesign of the existing protection systems of all typical European MV and LV grids**. Furthermore, with this positive and negative sequence voltage support strategy, the unbalanced faults on a lower voltage level have no significant impact on the higher voltage levels and the remaining SGs don't experience additional stress. **It can be concluded that the positive and negative sequence voltage support during unbalanced faults has many benefits** in scenarios with a high share of CBDG and little conventional generation. Injecting negative sequence reactive currents does limit the positive sequence current that can be injected, including the active power in some cases. This reduction of active power transfer was no problem in the case studies, but a final strategy in scenarios with a very high share of CBDG should also include an active power / frequency control by CBDG units. This topic is discussed further in section 6.4.

6.3 Recommendations to Stakeholders

Based on the research results of this work, following recommendations can be made:

- For **grid operators**, it is recommended to refuse converter based units to only provide positive sequence voltage support and to block the negative sequence currents during unbalanced faults. This approach boosts the voltages in the healthy phases and leads to additional stress on the SGs in the system. In grids with sufficient conventional generators, that naturally provide negative sequence voltage support (and high fault currents) during unbalanced faults, it is even a better option to not provide any voltage support during unbalanced faults, i.e. inject no additional reactive currents. A better approach is to require positive and negative sequence voltage support, or at least to require that this voltage support can be activated later. When the share of CBDG units increases, it will be beneficial to have this voltage support.
- For **manufacturers of CBDG units**, e.g. type 4 WTs, large PV installations, HVDC transmission systems, it is recommended to design CBDG units that can tolerate certain levels of power oscillations during unbalanced faults. They should give a clear view on technical constraints or additional costs of these levels of power oscillations. The positive and negative sequence voltage support strategy has many advantages for the

grid. Only when alternative strategies are technically required for the FRT of the CBDG units, it is worth considering these alternative strategies and designing other, costly measures to mitigate the disadvantages for the grid.

- For the **standards setting organisations**, it is recommended to find a general agreement on standards for the fault behaviour of CBDG units during unbalanced faults. The positive and negative sequence voltage support strategy should be a start for this discussion. However, it is possible that some aspects can be optimised. E.g. a voltage source behaviour could be beneficial for determining the priority between active and reactive current injections and for decreasing the response time of the CBDG units. These topics are discussed further in the next section.
- For **software developers**, it is recommended to implement a simplified calculation method that can take the fault behaviour of CBDG units into account. Present-day short-circuit calculation methods, e.g. according to IEC 60909 [86], are not suitable for scenarios with a high share of CBDG. More advanced simulation methods can accurately model these scenarios. However, they require detailed information, that is not always available, on all system elements and they are computationally intensive for larger systems. The suggested ILNEM can be considered as a simplified calculation method when it is capable to model the fault behaviour of future power systems during both balanced and unbalanced faults.

6.4 Future Work

During this work, several issues were identified that need further optimisation or further research.

Whenever the share of CBDG is so high that the number of SGs in the system is limited, the (fault) current contribution strategies of the CBDG units have a large impact. **The inertia of the system and the frequency stability will also determine the fault response that is required by the CBDG units**. Due to the current limitation, **the required active power also influences the possible positive and negative sequence voltage support**. In order to provide a certain positive sequence active current, it is possible that the positive and negative sequence reactive currents have to be reduced. However, when the fault currents remain high, the voltage change is only significant in a limited region of the network and the CBDG units in other regions in the network have more margin to supply active power for the frequency control. It is also expected that the load requirements drop during serious faults as some

loads decouple from the system. On the other hand, some loads may require more active current to obtain the same power during lower voltages, leading to higher active current requirements. The evaluation of these issues is not possible with the suggested ILNEM calculations, although the active power balance is taken into account. RMS, dynamic phasor or EMT simulations could be applied. This study also requires accurate load models during (un)balanced voltage dips, over a wide voltage range. These models are currently not available and have to be developed as well.

As indicated in chapter 2, the control of the negative sequence current injection during low negative sequence voltages is a challenge. When only positive sequence voltages are generated, which can be accomplished by removing the feed-forward of the negative sequence grid voltage in the control loop, the CBDG units can inject negative sequence currents during low negative sequence voltages. However, in this case, the injection is not controlled, but is determined by the negative sequence voltage and the filter impedance. An optimisation of the PLL for low negative sequence voltages, as indicated in section 2.4.1, or in general, **an optimisation of the whole control system for low negative sequence voltages** could obtain a controlled negative sequence current injection during low negative sequence voltages and thus reduce the deadband that is required for the control systems described in chapter 2.

Although type 3 WTs are not treated in this work, chapter 5 mentions that their **DFIGs naturally inject negative sequence currents during unbalanced faults**. The equivalent negative sequence reactance is relatively low, leading to a relatively strong reduction of the negative sequence voltages, i.e. they naturally provide a high negative sequence voltage support. When there are many type 3 WTs in the grid, the negative sequence voltages will be lower and the CBDG units can, within their current limit, inject relatively more positive sequence current. **The exact benefits of a combination of different DG types could be investigated on a larger scale**.

The control of CBDG units can interfere with the fault detection, as the voltage support standards require rise times of 30 ms and settling times of 60 ms. Compared to the instantaneous, natural response of SGs, this is relatively slow as some protection relays make decisions within this time frame. Therefore, **it should be verified whether this causes problems in real situations**. If this is the case, it should be investigated whether the response of the CBDG units can be made faster or whether the detection and response time of the relays can be increased. Studying these issues requires detailed models of the relays and EMT simulations.

Appendix A

Phasor and Space Vector Relations

First, this appendix clarifies the sign conventions that are used in this dissertation. Then, section A.2 explains the relationship between the current and voltage phasors, the space vectors and the results obtained by the calculation method from chapter 3, that are expressed in phase coordinates. The equations that allow to study the (variable) power transfer during unbalanced faults, are explained in section A.3. Small letters represent p.u. values, capitals represent normal values.

A.1 Sign Conventions

This dissertation uses the generator sign convention from [137] for all generators unless explicitly stated otherwise (e.g. when both generation and loads are listed in the same table). Likewise, for loads the load sign convention from [137] is used. This load sign convention is the same as the passive sign convention mentioned in [149]. This sign convention is called passive as, with this convention, passive elements absorb a positive real power. The generator sign convention is then the active sign convention. Both conventions are illustrated in Figure A.1. The convention of the voltage arrows used in this dissertation is also illustrated in this figure.

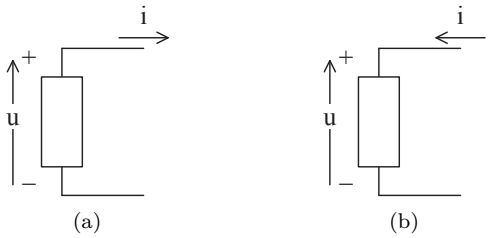


Figure A.1: (a): active sign convention or generator sign convention and (b): passive sign convention or load sign convention.

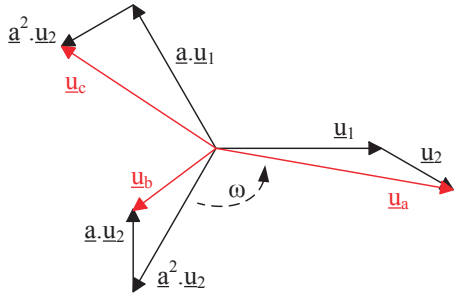


Figure A.2: Positive and negative sequence components and their composition to the total phase values (without zero sequence)

A.2 Symmetrical Components

This section explains the concepts and representations of symmetrical components that are used in this dissertation. Symmetrical components have been described in great detail in literature since the original paper of Fortescue [150]. A good overview of the symmetrical components in the time domain, including the relationship between symmetrical components, the Clarke transformation (to the two axis stationary frame: $abc \rightarrow \alpha\beta$) and the Park transformation (to the synchronously rotating frame: $\alpha\beta \rightarrow dq$) is given in [151]. As this work considers three-phase CBDG units, without neutral connection, the sources cannot inject zero sequence currents. In addition, the step-up transformer usually blocks the zero sequence voltages coming from the grid (e.g. delta-wye transformer). Therefore, the description here is limited to positive and negative sequence.

Phasors are indicated with underlined symbols. The real and imaginary part are

indicated with the indices r and i. Phasors always rotate synchronously with the fundamental frequency. Figure A.2 shows positive and negative sequence phasors and their composition to the total phasor values (here for the voltage phasors, but also valid for the current phasors). These are calculated based on:

$$\begin{bmatrix} \underline{u}_0 \\ \underline{u}_1 \\ \underline{u}_2 \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} 1 & 1 & 1 \\ 1 & \underline{a} & \underline{a}^2 \\ 1 & \underline{a}^2 & \underline{a} \end{bmatrix} \cdot \begin{bmatrix} \underline{u}_a \\ \underline{u}_b \\ \underline{u}_c \end{bmatrix} \tag{A.1a}$$

$$\begin{aligned} \underline{u}_1 &= \frac{1}{3} \left(\underline{u}_a + a \cdot \underline{u}_b + a^2 \cdot \underline{u}_c \right) \\ &= u_{1r} + j \cdot u_{1i} \\ &= u_1 \cdot e^{j \cdot \theta_1} \end{aligned} \tag{A.1b}$$

$$\begin{aligned} \underline{u}_2 &= \frac{1}{3} \left(\underline{u}_a + a^2 \cdot \underline{u}_b + a \cdot \underline{u}_c \right) \\ &= u_{2r} + j \cdot u_{2i} \\ &= u_2 \cdot e^{j \cdot \theta_2} \end{aligned} \tag{A.1c}$$

where $\underline{a} = e^{j \cdot 120^\circ}$ and $\underline{u}_{a,b,c}$ the line-to-ground voltage phasors.

For the time-varying line-to-ground voltages of the phases, this results in:

$$U_a(t) = \sqrt{2} \cdot U_{\text{nom}} \cdot \left(u_1 \cdot \cos\left(\omega t + \theta_1\right) + u_2 \cdot \cos\left(\omega t + \theta_2\right) \right) \tag{A.2a}$$

$$U_b(t) = \sqrt{2} \cdot U_{\text{nom}} \cdot \left(u_1 \cdot \cos\left(\omega t - \frac{2\pi}{3} + \theta_1\right) + u_2 \cdot \cos\left(\omega t + \frac{2\pi}{3} + \theta_2\right) \right) \tag{A.2b}$$

$$U_c(t) = \sqrt{2} \cdot U_{\text{nom}} \cdot \left(u_1 \cdot \cos\left(\omega t + \frac{2\pi}{3} + \theta_1\right) + u_2 \cdot \cos\left(\omega t - \frac{2\pi}{3} + \theta_2\right) \right) \tag{A.2c}$$

Space vectors are indicated with the $\angle$ symbol ($\angle 0$ for a fixed frame $\alpha\beta$). Also the total space vector can be expressed based on the positive and negative sequence components [39]:

$$
\begin{aligned}
\underline{u}^{\angle 0} &= u_\alpha + j \cdot u_\beta \qquad (A.3)\\
&= \frac{2}{3}\left(u_a + \underline{a} \cdot u_b + \underline{a}^2 \cdot u_c\right)\\
&= \frac{1}{3}\left(\underline{u}_a^{\angle 0} + \left(\underline{u}_a^{\angle 0}\right)^* + \underline{a} \cdot \left(\underline{u}_b^{\angle 0} + \left(\underline{u}_b^{\angle 0}\right)^*\right) + \underline{a}^2 \cdot \left(\underline{u}_c^{\angle 0} + \left(\underline{u}_c^{\angle 0}\right)^*\right)\right)\\
&= \frac{1}{3}\left(\underline{u}_a^{\angle 0} + \underline{a} \cdot \underline{u}_b^{\angle 0} + \underline{a}^2 \cdot \underline{u}_c^{\angle 0}\right) + \frac{1}{3}\left(\left(\underline{u}_a^{\angle 0}\right)^* + \underline{a} \cdot \left(\underline{u}_b^{\angle 0}\right)^* + \underline{a}^2 \cdot \left(\underline{u}_c^{\angle 0}\right)^*\right)\\
&= \underline{u}_1^{\angle 0} + \left(\underline{u}_2^{\angle 0}\right)^*\\
&= (u_{1\alpha} + j \cdot u_{1\beta}) + (u_{2\alpha} + j \cdot u_{2\beta})^*\\
&= (u_{1r} + j \cdot u_{1i}) \cdot e^{j\omega t} + (u_{2r} + j \cdot u_{2i})^* \cdot e^{-j\omega t}
\end{aligned}
$$

When looking at the transformation of the phasor calculations in symmetrical components (A.1), these results can be related directly to the space vector (A.3), so $\underline{u}_1^{\angle 0} = \underline{u}_1 \cdot e^{j\omega t}$).

The total space vector is shown in Figure A.3. The path of the space vector is a circle when there are only positive sequence components, but it becomes an ellipse when there are also negative sequence components.

A.3 Instantaneous Power

While the instantaneous power relationships are well known from literature, the calculation in phasor coordinates requires that the mathematically correct description of the total space vector is used, as defined in section A.2: the sum of a positive sequence space vector rotating counterclockwise and the complex conjugate of a negative space sequence vector rotating clockwise [39, 151]. Some papers [59] consider the total space vector as a positive sequence space vector rotating counterclockwise and a negative space sequence vector rotating clockwise. This explains the different signs of the equations compared to some papers [59] and allows to easily relate the negative sequence space vector with the negative sequence quantities calculated from the phasor calculations (i.e. they are the same, as explained in section A.2).

In absence of zero sequence components, and with only fundamental frequency positive and negative sequence components, the instantaneous power theory

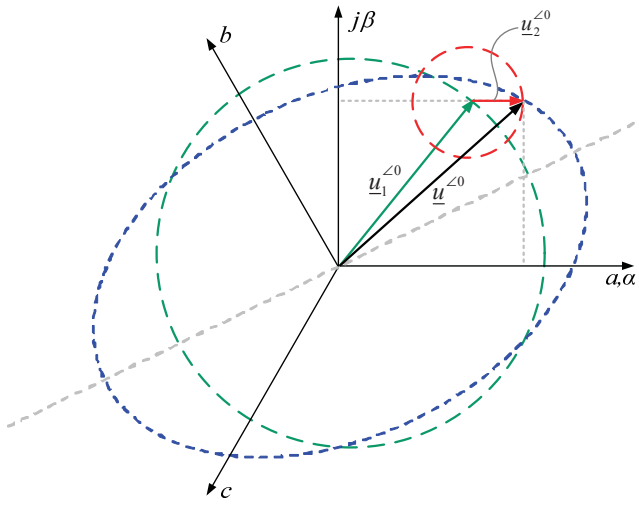


Figure A.3: Path of the total space vector with positive and negative sequence components. (source: [39])

results in six power components (A.4). According to the interpretation of Aredes [17, 141], in a three-phase system, the variable frequency p components represent a power exchange in and out of the system, while the q components indicate a power exchange between the phases. It is therefore common to try to minimise the variable p components to limit power ripples for the sources, as the q components do not influence the power ripple for the source (e.g. DC bus of converter, shaft of turbine). The p components can be studied based on the phasor calculations with (A.5).

$$\begin{aligned} \underline{s} &= \underline{u}^{\angle 0} \cdot \underline{i}^{*\angle 0} \\ &= p + j \cdot q \end{aligned} \tag{A.4a}$$

$$p = p_0 + p_{c2} \cdot cos(2\omega t) + p_{s2} \cdot sin(2\omega t) \tag{A.4b}$$

$$q = q_0 + q_{c2} \cdot cos(2\omega t) + q_{s2} \cdot sin(2\omega t) \tag{A.4c}$$

$$p_0 = u_{1r} \cdot i_{1r} + u_{1i} \cdot i_{1i} + u_{2r} \cdot i_{2r} + u_{2i} \cdot i_{2i} \tag{A.5a}$$

$$p_{c2} = u_{1r} \cdot i_{2r} - u_{1i} \cdot i_{2i} + u_{2r} \cdot i_{1r} - u_{2i} \cdot i_{1i} \tag{A.5b}$$

$$p_{s2} = -u_{1r} \cdot i_{2i} - u_{1i} \cdot i_{2r} - u_{2r} \cdot i_{1i} - u_{2i} \cdot i_{1r} \tag{A.5c}$$

$$p_{var} = |p_{c2} + j \cdot p_{s2}| = \sqrt{p_{c2}^2 + p_{s2}^2} \tag{A.5d}$$

$$q_0 = -u_{1r} \cdot i_{1i} + u_{1i} \cdot i_{1r} + u_{2r} \cdot i_{2i} - u_{2i} \cdot i_{2r} \tag{A.5e}$$

$$q_{c2} = u_{1r} \cdot i_{2i} + u_{1i} \cdot i_{2r} - u_{2r} \cdot i_{1i} - u_{2i} \cdot i_{1r} \tag{A.5f}$$

$$q_{s2} = u_{1r} \cdot i_{2r} - u_{1i} \cdot i_{2i} - u_{2r} \cdot i_{1r} + u_{2i} \cdot i_{1i} \tag{A.5g}$$

Example

To illustrate these formulas, a small example is considered.

Assume $\underline{u}_1 = 0.573 \cdot e^{j \cdot 27^\circ}$, $\underline{u}_2 = 0.383 \cdot e^{j \cdot -153.7^\circ}$, $\underline{i}_1 = 0.695 \cdot e^{j \cdot -56.8^\circ}$ and $\underline{i}_2 = 0.503 \cdot e^{j \cdot -63.7^\circ}$. Based on these positive and negative sequence currents and voltages, the currents and voltages in phase coordinates are calculated. Afterwards, the time-varying power in each phase is calculated based on the time-varying current and voltage:

$$p_i(t) = u_i(t) \cdot i_i(t) \qquad i = a, b, c \tag{A.6}$$

Figure A.4 shows the power components in each phase, the sum of these three components, i.e. the three-phase power $p_{3\phi}$, the average power p_0 based on (A.5a) (solid horizontal line) and the variable power $p_0 \pm p_{\text{var}}$ based on (A.5d) (dashed horizontal lines). All values are expressed in p.u. referred to the three-phase nominal power. From this example, it is clear that the formulas (A.5) allow to study the instantaneous power of positive and negative sequence currents and voltages without requiring EMT simulations.

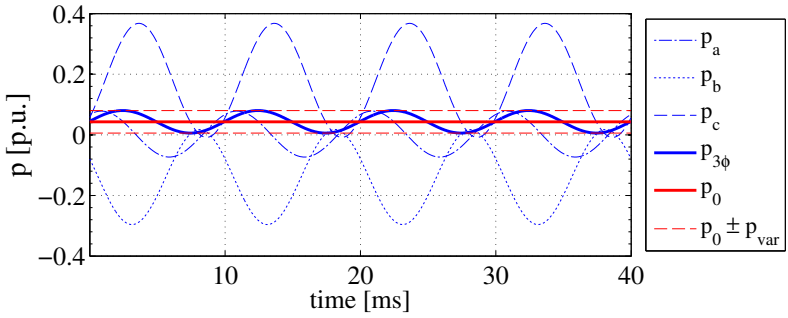


Figure A.4: Illustration of the instantaneous power formulas

Appendix B

Test System Data

This appendix lists the system data for the test systems used in chapter 3 (Figure 3.12), chapter 4 (Figure 4.5) and chapter 5 (Figure 5.15).

Table B.1: Generator data

		SG1	**SG2**	**SG3**
S_{nom} [MVA]		247.5	192	128
U_{nom} [kV]		16.5	18	13.8
Synchronous	x_d	0.361	1.720	1.68
reactance [p.u.]	x_q	0.240	1.660	1.610
Transient	x'_d	0.150	0.230	0.232
reactance [p.u.]	x'_q	/	0.378	0.320
Subtransient	x''_d	0.129	0.212	0.214
reactance [p.u.]	x''_q	0.159	0.212	0.214
Transient open	T'_{d0}	8.96	6	5.89
circuit time constant [s]	T'_{q0}	/	0.535	0.6
Subtransient open	T''_{d0}	0.05	0.035	0.05
circuit time constant [s]	T''_{q0}	0.09	0.029	0.05
Inertia constant [s]	H	9.552	3.333	2.352

Table B.2: Transformer data

	T_1	**T_2**	**T_3**	**PT**	**DT**
S_{nom} [MVA]	250	200	150	200	50
U_{prim} [kV]	230	230	230	230	110
U_{sec} [kV]	16.5	18	13.8	110	15
u_k [%]	14.4	12.5	8.79	20	15
Vector group	Yd5	Yd5	Yd5	Yy0	Yd11

Table B.3: Line data

line	**4-5**	**5-7**	**7-8**	**8-9**	**6-9**	**4-6**	**110 kV**
R_1 [Ω]	1.32	4.23	1.12	1.57	5.16	2.25	2.38
X_1 [Ω]	11.24	21.29	9.52	13.33	22.48	12.17	7.74
R_0 [Ω]	4.63	14.81	3.93	5.51	18.05	7.87	6.18
X_0 [Ω]	39.34	74.52	33.33	46.66	78.69	42.58	27.64
B [µS]	83.2	144.6	70.4	98.8	169.2	74.7	0

Appendix C

Additional Results

This appendix lists the additional results for the case studies in chapter 5.

C.1 Additional Results for Section 5.3

C.1.1 Results Single-Line-to-Ground Faults (Section 5.3.5)

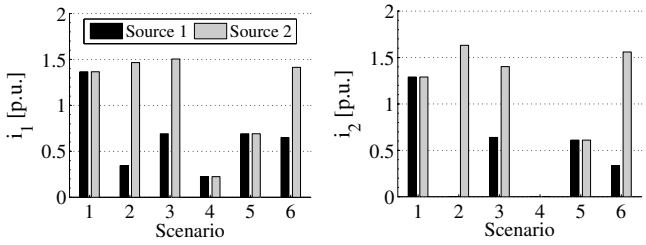


Figure C.1: Single-line-to-ground fault F1: (a) positive sequence current contribution i_1 and (b) negative sequence current contribution i_2 of source 1 and 2

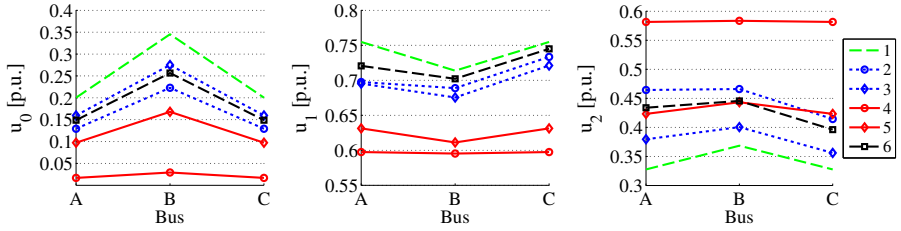


Figure C.2: Single-line-to-ground fault F1: (a) zero sequence voltage u_0, (b) positive sequence voltage u_1 and (c) negative sequence voltage u_2 at bus A, B and C

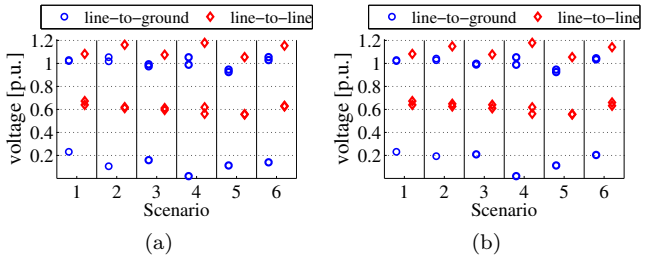


Figure C.3: Single-line-to-ground fault F1: (a) Voltages at bus A and (b) at bus C

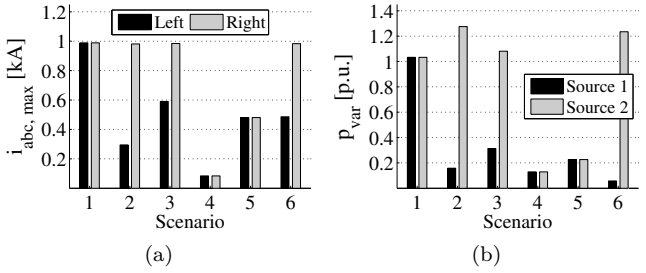


Figure C.4: Single-line-to-ground fault F1: (a) Maximum phase current on both sides of the fault and (b) the power oscillation of both sources

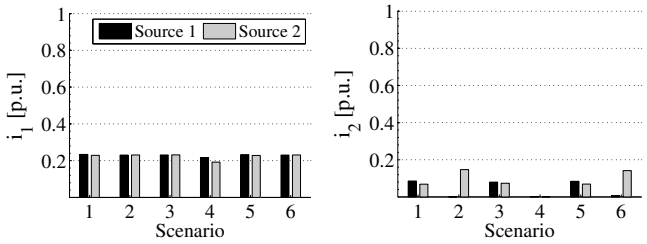


Figure C.5: Single-line-to-ground fault F2: (a) positive sequence current contribution i_1 and (b) negative sequence current contribution i_2 of source 1 and 2

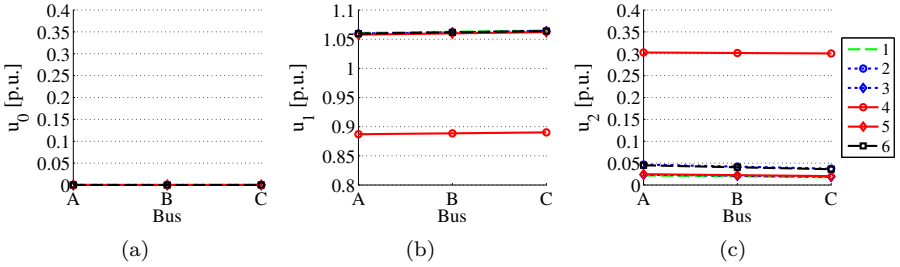


Figure C.6: Single-line-to-ground fault F2: (a) zero sequence voltage u_0, (b) positive sequence voltage u_1 and (c) negative sequence voltage u_2 at bus A, B and C

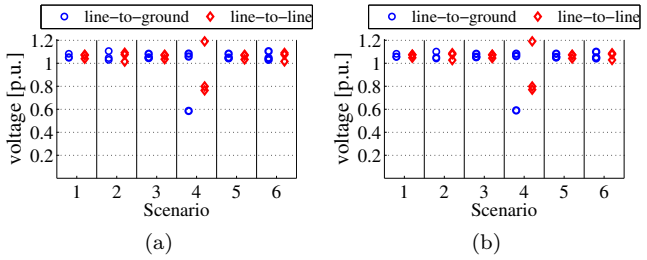


Figure C.7: Single-line-to-ground fault F2: (a) Voltages at bus A and (b) at bus C

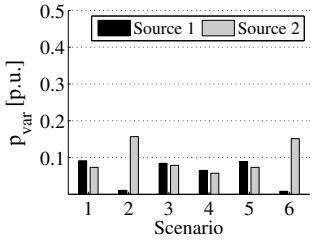


Figure C.8: Single-line-to-ground fault F2: the power oscillation of both sources

C.1.2 Results Two-Lines-to-Ground Faults (Section 5.3.6)

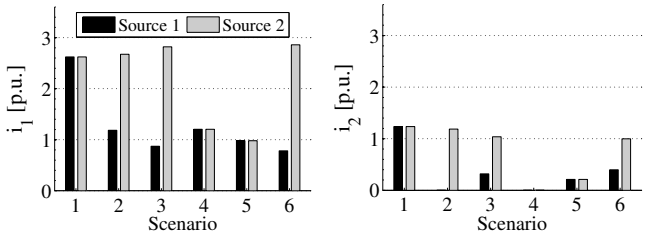


Figure C.9: Two-lines-to-ground fault F1: (a) positive sequence current contribution i_1 and (b) negative sequence current contribution i_2 of source 1 and 2

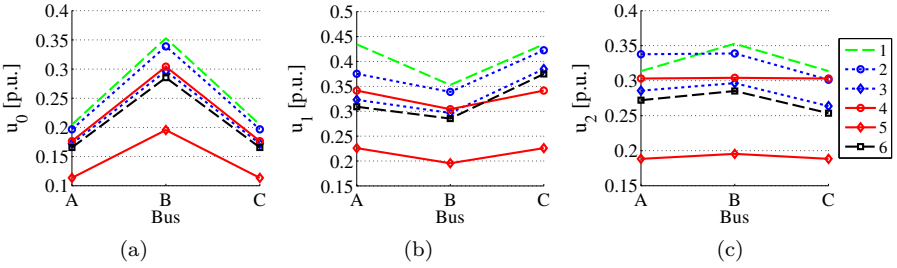


Figure C.10: Two-lines-to-ground fault F1: (a) zero sequence voltage u_0, (b) positive sequence voltage u_1 and (c) negative sequence voltage u_2 at bus A, B and C

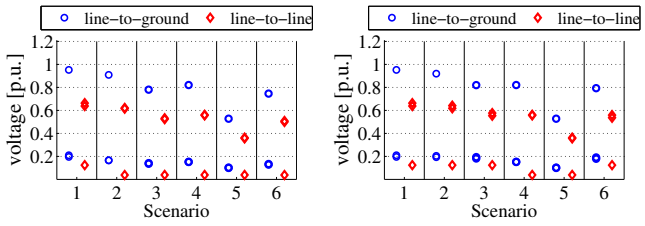


Figure C.11: Two-lines-to-ground fault F1: (a) Voltages at bus A and (b) at bus C

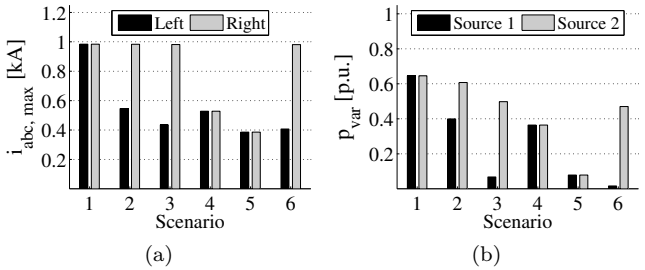


Figure C.12: Two-lines-to-ground fault F1: (a) Maximum phase current on both sides of the fault and (b) the power oscillation of both sources

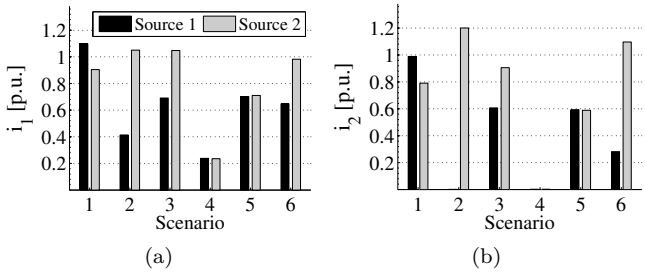
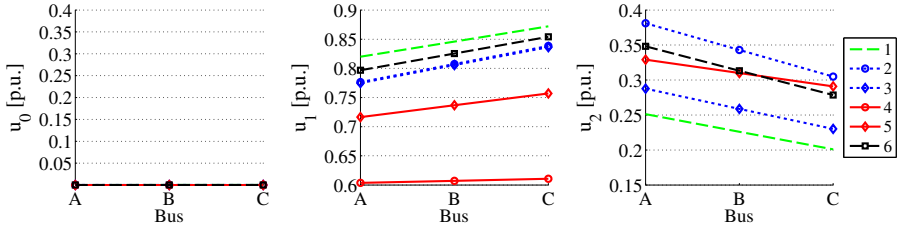
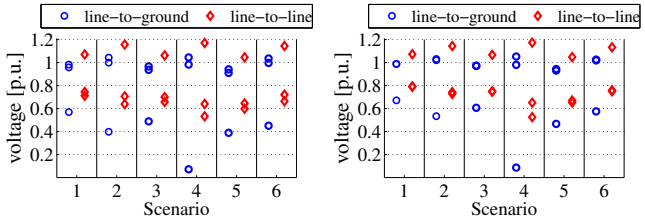


Figure C.13: Two-lines-to-ground fault F2: (a) positive sequence current contribution i_1 and (b) negative sequence current contribution i_2 of source 1 and 2



(a) (b) (c)

Figure C.14: Two-lines-to-ground fault F2: (a) zero sequence voltage u_0, (b) positive sequence voltage u_1 and (c) negative sequence voltage u_2 at bus A, B and C



(a) (b)

Figure C.15: Two-lines-to-ground fault F2: (a) Voltages at bus A and (b) at bus C

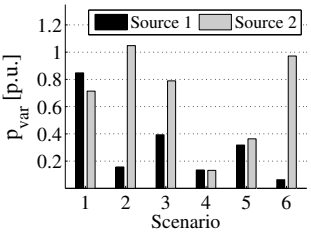


Figure C.16: Two-lines-to-ground fault F2: the power oscillation of both sources

C.2 Additional Results for Section 5.4

C.2.1 Results Single-Line-to-Ground Faults (Section 5.4.4)

Table C.1: Results for the single-line-to-ground faults on the test system (1)

Scenario	**Fault**	$\mathbf{I_{sc}}$ [kA]	**Source 1** $\mathbf{p_{var}}$ [p.u.]	$\mathbf{I_{1q}}$ [kA]	$\mathbf{I_{2q}}$ [kA]
SG-n	F1	4.0	0.70	-8.5	7.8
SG-n	F2	5.0	0.43	-4.7	4.1
SG-n	F3	1.0	0.01	-0.5	0.1
SG-p	F1	2.8	1.01	-8.4	11.2
SG-p	F2	4.0	0.76	-4.7	7.3
SG-p	F3	0.9	0.03	-0.5	0.2
VSC-n	F1	3.4	0.33	-5.4	5.0
VSC-n	F2	4.9	0.36	-4.1	3.7
VSC-n	F3	1.0	0.01	-0.4	0.1
VSC-np	F1	1.8	0.34	-3.4	5.1
VSC-np	F2	3.3	0.48	-3.5	5.4
VSC-np	F3	0.9	0.03	-0.4	0.2
VSC-p	F1	1.3	0.15	-0.7	0.0
VSC-p	F2	2.3	0.12	-0.8	0.0
VSC-p	F3	1.0	0.01	-0.4	0.0
VSC-n-low-k	F1	3.2	0.32	-5.4	5.0
VSC-n-low-k	F2	4.4	0.29	-3.7	3.3
VSC-n-low-k	F3	1.0	0.01	-0.5	0.1
VSC-p-load2	F1	0.7	0.20	0.6	0.0
VSC-p-load2	F2	1.3	0.19	0.0	0.0
VSC-p-load2	F3	1.0	0.01	-0.4	0.0

Table C.2: Results for the single-line-to-ground faults on the test system (2)

Scenario	**Fault**	**DG sub 1A** $\mathbf{p_{var}}$ [p.u.]	**DG sub 1B** $\mathbf{p_{var}}$ [p.u.]	**DG sub 2B** $\mathbf{p_{var}}$ [p.u.]
SG-n	F1	0.35	0.36	0.31
SG-n	F2	0.35	0.27	0.21
SG-n	F3	0.01	0.07	0.00
SG-p	F1	0.22	0.22	0.17
SG-p	F2	0.22	0.26	0.11
SG-p	F3	0.01	0.02	0.00
VSC-n	F1	0.31	0.31	0.28
VSC-n	F2	0.33	1.09	0.95
VSC-n	F3	0.01	0.07	0.00
VSC-np	F1	0.21	0.25	0.20
VSC-np	F2	0.18	0.20	0.13
VSC-np	F3	0.01	0.02	0.00
VSC-p	F1	0.30	0.36	0.26
VSC-p	F2	0.29	0.33	0.18
VSC-p	F3	0.01	0.02	0.01
VSC-n-low-k	F1	0.24	0.24	0.25
VSC-n-low-k	F2	0.24	0.23	0.17
VSC-n-low-k	F3	0.01	0.05	0.01
VSC-p-load2	F1	0.10	0.11	0.12
VSC-p-load2	F2	0.10	0.12	0.10
VSC-p-load2	F3	0.01	0.01	0.01

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List of Publications

First, the publications that are directly related to the content of this dissertation are listed. Afterwards, publications related to project work, guiding master thesis students, helping colleagues and my master thesis are listed.

Publications Directly Related to this Dissertation

Reviewed Journals

T. Neumann, T. Wijnhoven, G. Deconinck, and I. Erlich, "Enhanced Dynamic Voltage Control of Type 4 Wind Turbines during Unbalanced Grid Faults," Accepted for publication in *IEEE Transactions on Energy Conversion*, 2015.

International Conferences

T. Neumann, T. Wijnhoven, G. Deconinck, and I. Erlich, "Response of an AC-DC Hybrid Transmission System to Faults in the AC Network," in *IEEE PES General Meeting (Best Paper Session on Cyber Security, Stability, and Protection)*, 2015, p. 5.

T. Wijnhoven, J. Tant, T. Neumann, I. Erlich, and G. Deconinck, "Influence of Voltage Support by Converter Based Distributed Generation on the Short-Circuit Power," in *IEEE PowerTech*, 2015, p. 6.

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T. Wijnhoven and G. Deconinck, "Flexible Fault Current Contribution with Inverter Interfaced Distributed Generation," in *IEEE PES General Meeting*, 2013, p. 5.

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Other Publications

International Conferences

N. Efkarpidis, T. Wijnhoven, C. Gonzalez de Miguel, T. De Rybel, J. Driesen, "Coordinated Voltage Control Scheme for Flemish LV Distribution Grids Utilizing OLTC Transformers and D-STATCOM's," in *12th IET International Conference on Developments in Power System Protection (DPSP)*, 2014, p. 6.

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Curriculum Vitae

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1997–2003	Secondary school Science-Mathematics (8h) Heilig Hartinstituut, Heverlee
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